Getting Started with the TS83102G0B 10-bit 2 Gsps ADC and the TS81102G0 1:4/8 DMUX

Introduction

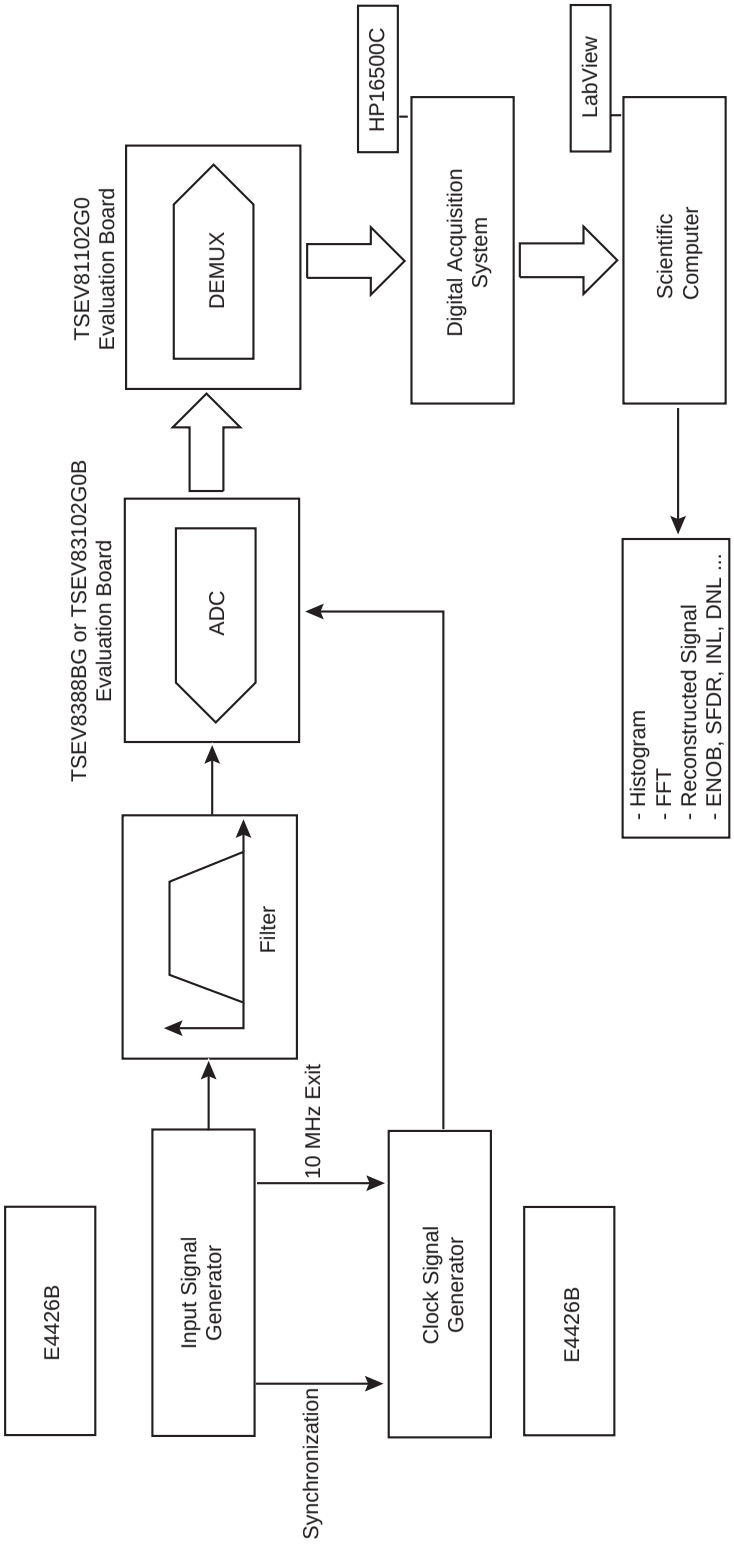
The aim of this Application Note is to help the user set up the test bench using Atmel's TS83102G0B 10-bit 2 Gsps ADC and TS81102G0 1:4/8 DMUX evaluation boards. It first gives a description of the test bench used in Atmel's laboratory, provides recommendations on how to connect all the components together and finally describes in detail the test procedure that should be followed to rapidly evaluate Atmel broadband data conversion devices.

TS83102G0B and TS81102G0 Evaluation Boards

Application Note

Rev. 5351A-BDC-10/03

Figure 1. Test bench

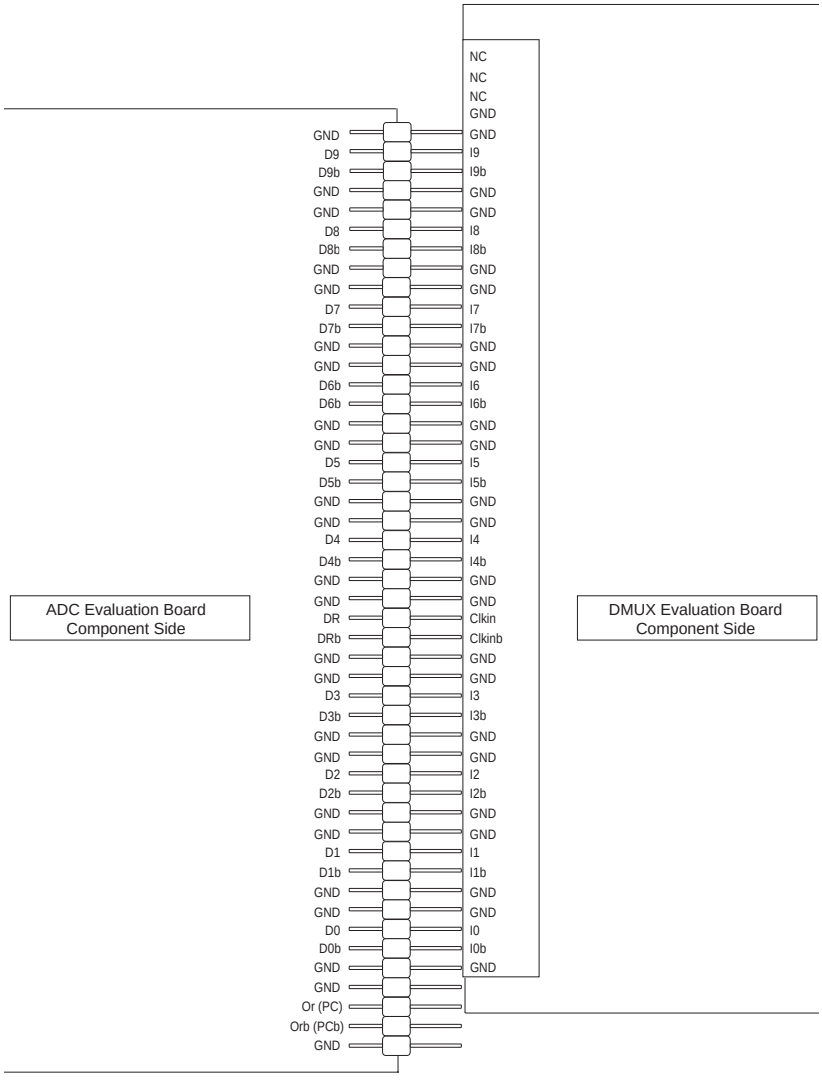


Interfacing the ADC and DMUX Evaluation Boards

Settings

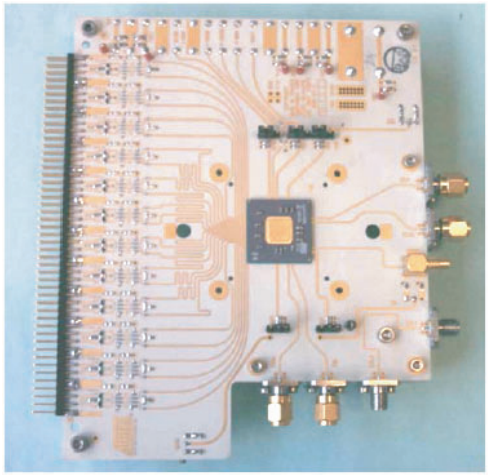
In Figure 2, there is an offset of 4 rows between the ADC output connector and the DMUX input connector.

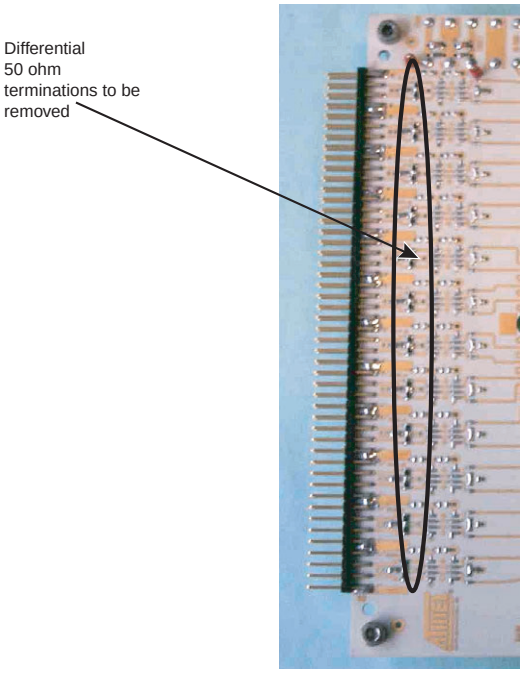
Figure 2. Evaluation Boards (ADC in CBGA Package)



Since both the ADC data outputs are on-board 50 Ω differentially terminated and the DMUX input buffers are on-chip 50 Ω differentially terminated, it may be necessary to remove the extra termination at the ADC end when the ADC board is to be plugged to the DMUX board.

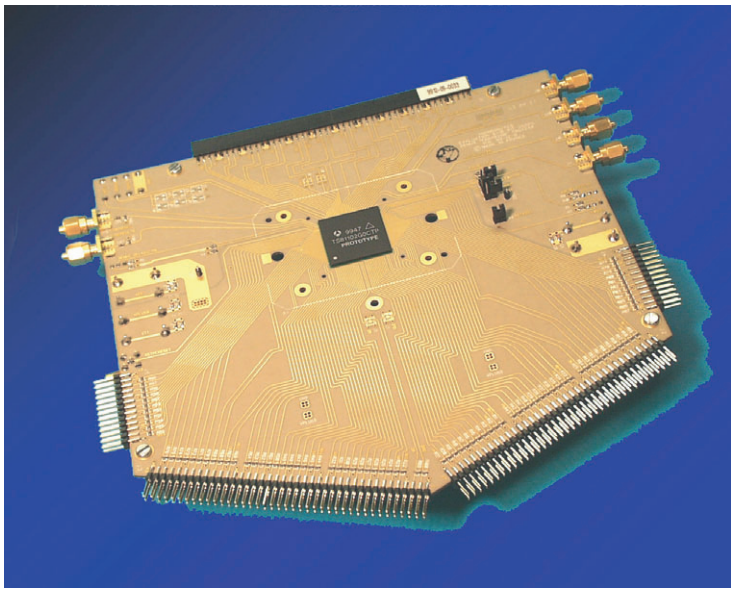
Figure 3. Boards without Digital Output Buffers

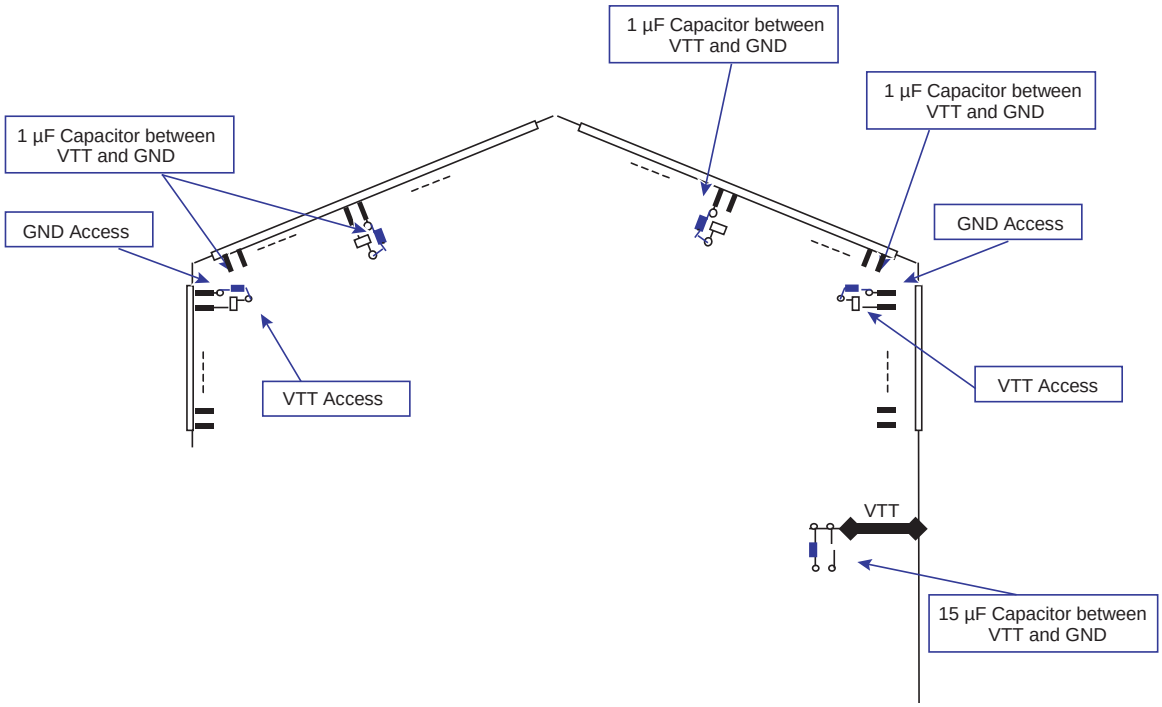




It may be necessary to add extra decoupling capacitors at the DMUX output between V_{TT} and ground: 4 capacitors of 1 µF are recommended with 1 capacitor of 15 µF.

Figure 4. DMUX Evaluation Board





Other Settings

- DMUX jumpers[1]
  - BIST: jumper OUT
  - NBBIT: jumper OUT
  - CLKINTYPE: jumper ON
  - RATIOSEL: jumper ON (for 1:8 ratio)

- Power supplies

  ADC
  - V_{EE} = D_{VEE} connected to -5 V supply
  - V_{CC} connected to 5 V supply
  - V_{PLUSD} = GND[2]

  DMUX
  - V_{EE} connected to -5 V supply
  - V_{CC} connected to 5 V supply
  - V_{TT} connected to -2 V in ECL mode

  All grounds have to be connected together.

Notes:
1. BIST jumper ON = BIST active
   NBBIT jumper ON = 8-bit
   CLKINTYPE jumper OUT = DR mode
   RATIOSEL jumper OUT = 1:4 ratio
2. The DMUX is specified to only accept ECL levels at its inputs but, when associated with Atmel's ADC, it is not necessary to set the ADC in ECL output format (for example, to set V_{PLUSD} to -0.8 V) since the DMUX can accept the levels coming from the ADC when V_{PLUSD} (ADC) is tied to ground. However, you still have the opportunity to have ECL levels at the ADC output. In this case, the V_{PLUSD} voltage has to be connected to ground via a 5.2 Ω shunt resistor.

Connecting the Logic Analyzer

Finally, once the ADC and DMUX boards are connected and ready for operation, the last step before power up is to connect the logic analyzer probes to the DMUX outputs. It is recommended to have at least one of the DMUX ports fully connected to the logic analyzer in addition to the Data Ready signal from the DMUX, thus providing the synchronization clock for the logic analyzer.

Quick Start

Power Up Sequence

1. Apply the D_{VEE} = V_{EE} = -5 V power supplies (on both ADC and DMUX).
2. Turn on the V_{CC} = 5 V power supply (on both ADC and DMUX).
3. Supply V_{TT}.
4. All grounds have to be connected (as well as V_{PLUSD}: two options, either to -0.8 V via a 5.2 Ω shunt resistor to ground or directly to ground).
5. You can then apply the clock (0 dBm sinusoidal differential clock) and the analog input (-1 dBFS input level).
6. Finally, you need to perform an asynchronous reset on the DMUX.

The devices should now operate properly. The next section describes the test procedure to be followed so that the whole system works correctly and optimum results are obtained.

Test Procedure

DMUX Output Levels Setting

This first step is mandatory to match the logic analyzer threshold to the DMUX output levels in both DC and dynamic conditions.

Static Adjustment

Configuration

ADC and DMUX ON, logic analyzer ON.

1. The clock and analog input signals are active at the ADC input (the frequency of both signals has no importance but one could choose Fs = 2 Gsps and Fin close to Fs/2 for optimum settings). Perform an asynchronous reset on the DMUX and then release it to make the system operational and re-activate the asynchronous reset to freeze the outputs at their level at reset.

Note: Always choose Fs and Fin so that Fs/Fin = N/M, where N = number of samples (2^n) and M = number of cycles (must be an odd number).

2. While the asynchronous reset of the DMUX is active (held high), with a voltmeter measure the VOL and VOH levels of all the output bits of the DMUX and the Vref level of all ports.

Vref should be close to (VOL + VOH)/2. In a typical case, Vref is lower than (VOL + VOH)/2.

The logic analyzer threshold has to be set to the value obtained with (VOL+VOH)/2.

Notes:
1. The logic analyzer threshold is a very important parameter in a single-ended data acquisition. This is not the case when dealing with differential data acquisition (both Data and DataB are taken into account).
2. It is necessary to calibrate the logic analyzer with all the probes connected prior to the first acquisition.
3. Setting the threshold of the logic analyzer between -1.4 V and -1.6 V should satisfy the conditions for detection of the DMUX output data.

Dynamic Check

To make sure the previous value for the Logic Analyzer threshold is correct for both DC and dynamic domains, a dynamic test has to be performed.

1. From the last configuration, de-activate the asynchronous reset of the DMUX (the data should then run at the DMUX output).
2. With Fs = 2 Gsps and Fin close to Fs/2 (~ 1 GHz in Nyquist conditions), measure the VOL and VOH with an oscilloscope (eye diagram). The Vref value can also be checked with a voltmeter.
3. The obtained VOL, VOH and Vref values should be close to the ones found during the previous test. If not, we recommend you re-check the connection between the ADC and the DMUX boards:

- Is the data from the ADC properly sent to the DMUX?
- Perform another asynchronous reset on the DMUX and see what happens.
- Tune the DMUX swing adjust.

4. If you still cannot identify the source of your problem:

- Check the entire system again.
- Take down all your test conditions.

Finally, contact the hotline at hotline-bdc@gfo.atmel.com for support.

5. If the output swing (VOH - VOL) is too low for the Logic Analyzer to detect the DMUX outputs, then the DMUX swing adjust should be used. By tuning the swing adjust, you should be able to obtain satisfying values for VOL, VOH and Vref.

Note: The nominal setting for the swing adjust (SWIADJ = 0 V) of the DMUX should be suitable for a standard HP Logic Analyzer.

DMUX Delay Adjust

Once you are sure that the logic analyzer effectively detects the DMUX outputs, the next adjustment is the delay adjust of the DMUX (DMUXDelAdj).

1. Using the same configuration as previously described (Fs = 2 Gsps and Fin close to Fs/2), one can find the right DMUX delay to perform optimum synchronization between the ADC and the DMUX.

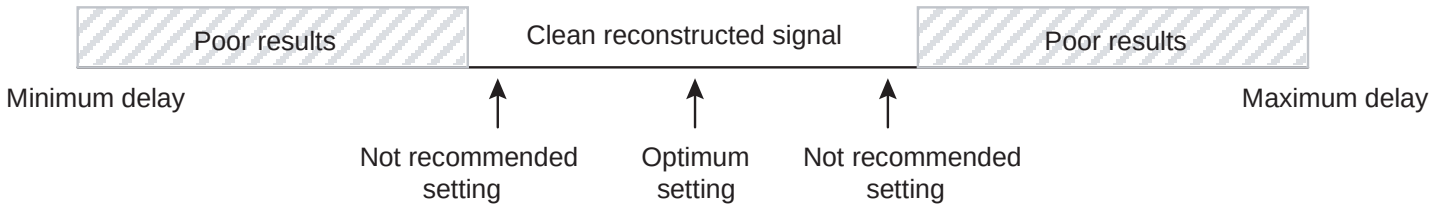
   For this setting, special care has to be taken with the sampling and input frequencies. In fact, the adjustment on the DMUX delay adjust depends on the sampling frequency. It does not depend on the input frequency, but the optimum setting for a given sampling frequency is achieved when the Nyquist condition is met, where Fin = Fs/2.

2. To find the right adjustment between the DMUX and ADC, it is recommended to cover the entire DMUX delay adjust range and check the reconstructed signal obtained for each delay.

   The optimum delay is the one which corresponds to a clean reconstructed signal with no glitch (it is possible that a whole range of delays is satisfactory).

   In addition, as illustrated in Figure 5, you should not choose a delay too close to an adjustment where the ADC gives poor results.

Figure 5. DMUX Delay Adjust



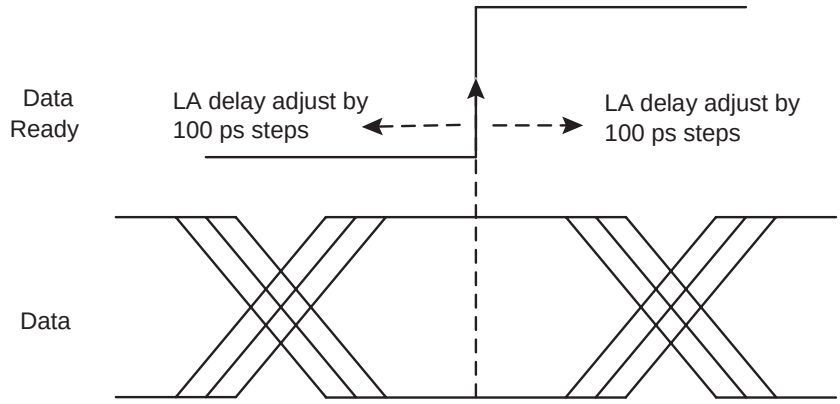
Note: It was observed that for Fs = 2 Gsps, the optimum setting was usually at the maximum of the delay adjust function (end course of the potentiometer, ~ 500 mV).

Logic Analyzer Delay Adjust

If the results are still not satisfactory (glitches on the reconstructed signal), the last adjustment to make is the Logic Analyzer delay.

1. By means of an oscilloscope, the eye diagram with the data and the Data Ready signal should be observed. In theory, the Data Ready signal should be right in the middle of the data but a small amount of skew may have made it shift to the right or left.
2. Fine tuning the logic analyzer delay may then be necessary to prop up the Data Ready signal in the middle of the data.

Figure 6. Logic Analyzer Delay Adjust



We then recommend you proceed as follows:

3. First, by 500 ps steps, change the logic analyzer delay to approximately find the "good" and "bad" zones (these are where the reconstructed signal shows many glitches)
4. Second, by 100 ps steps, fine-tune the logic analyzer delay until the reconstructed signal has no glitch and until the test gives satisfying dynamic results.

Typical results you should obtain are:

At Fs = 2 Gsps Fin = 1 GHz (-1 dBFS input level)

SFDR = -54 dBc

THD = -49 dB

SNR = 40 dB

ENOB = 6.5 bits

If you still do not obtain the expected results for the ADC, please contact the hotline for specific technical support at hotline-bdc@gfo.atmel.com

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
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Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

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