# Datasheet - *Preliminary Specification*

Features

- **Embedded e500 Book E-compatible Core Available up to 833 MHz**
    - **32-bit, Dual-issue, Superscalar, Seven-stage Pipeline**
    - **1850 MIPS at 800 MHz (Est. Dhrystone 2.1)**
    - **32 KB L1 Data and 32 KB L1 Instruction Cache with Line Locking Support**
    - **256 KB On-chip L2 Cache with Direct Mapped Capability**
    - **Enhanced Hardware and Software Debug Support**
    - **Memory Management Unit (MMU)**
    - **SIMD Extension with Single Precision Floating Point**
- **Two TSECs Supporting 10/100/1000 Mbps Ethernet (IEEE[®] 802.3, 802.3u, 802.3x, 802.3z, and 802.3 ac-compliant) with Two GMII/TBI/RGMII Interfaces**
- **166 MHz, 64-bit, 2.5V I/O, DDR SDRAM Memory Controller with Full ECC Support**
- **500 MHz, 8-bit, LVDS I/O, RapidIO Controller**
- **133 MHz, 64-bit, 3.3V I/O, PCI-X 1.0a/PCI 2.2 Bus Controller**
- **166 MHz, 32-bit, 3.3V I/O, Local Bus with Memory Controller**
- **Integrated Four-channel DMA Controller**
- **Interrupt Controller**
- **IEEE 1149.1 JTAG Test Access Port**
- **1.2V Core Voltage with 3.3V and 2.5V I/O**
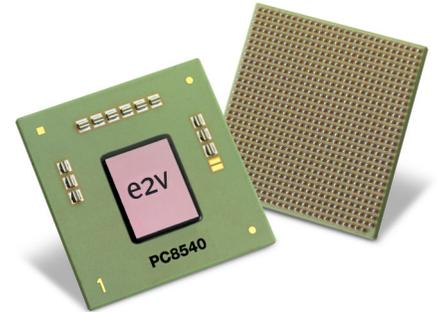
Description

The PC8540 contains a PowerPC[®] processor core. The PC8540 integrates a processor that implements the PowerPC architecture with system logic required for networking, storage, and general-purpose embedded applications. For functional characteristics of the processor, refer to the PC8540 Integrated Processor Preliminary Reference Manual.
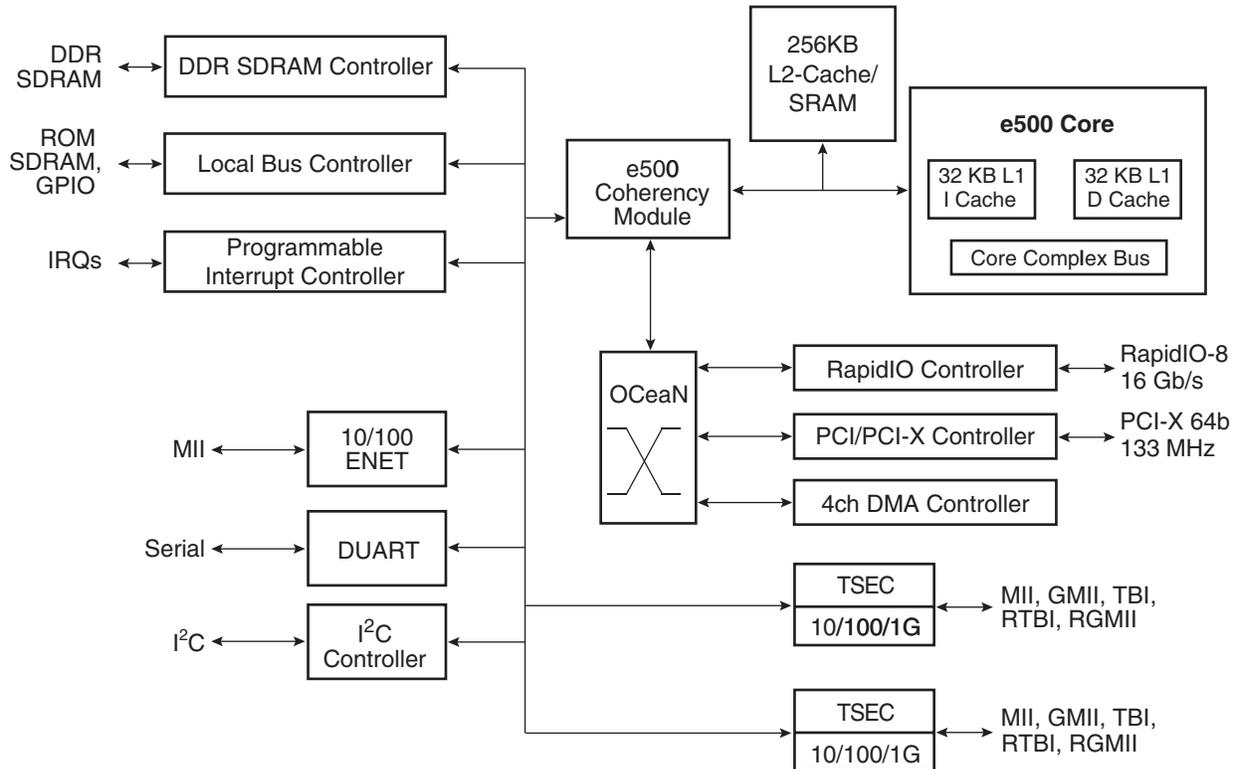
Screening/Quality/Packaging

- **T_J = -55°C, +125°C**
- **T_J = -40°C, +110°C**
- **783-pin HiTCE Package**

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1. Overview

The following section provides a high-level overview of the PC8540 features. Figure 1-1 shows the major functional units within the PC8540.

Figure 1-1. Block Diagram

1.1 Key Features

The following lists an overview of the PC8540 feature set.

- High-performance, 32-bit Book E-enhanced core that implements the PowerPC architecture
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis. Separate locking for instructions and data
  - Memory Management Unit (MMU) especially designed for embedded applications
  - Enhanced hardware and software debug support
- 256 Kbyte L2 cache/SRAM
  - Can be configured as follows:
    - Full cache mode (256-Kbyte cache)
    - Full memory-mapped SRAM mode (256-Kbyte SRAM mapped as a single 256 Kbyte block or two 128-Kbyte blocks)
    - Half SRAM and half cache mode (128-Kbyte cache and 128-Kbyte memory-mapped SRAM)
  - Full ECC support on 64-bit boundary in both cache and SRAM modes
  - Cache mode supports instruction caching, data caching, or both

- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing)
- Eight-way set-associative cache organization (1024 sets of 32-byte cache lines)
- Supports locking the entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions
- Global locking and flash clearing done through writes to L2 configuration registers
- Instruction and data locks can be flash cleared separately
- Read and write buffering for internal bus accesses
- SRAM features include the following:
  - I/O devices access SRAM regions by marking transactions as snoopable (global)
  - Regions can reside at any aligned location in the memory map
  - Byte accessible ECC is protected using read-modify-write transactions accesses for smaller than cache-line accesses.
- Address Translation and Mapping Unit (ATMU)
  - Eight local access windows define mapping within local 32-bit address space
  - Inbound and outbound ATMUs map to larger external address spaces
    - Three inbound windows plus a configuration window on PCI/PCI-X
    - Four inbound windows plus a default and configuration window on RapidIO
    - Four outbound windows plus default translation for PCI
    - Eight outbound windows plus default translation for RapidIO
- DDR memory controller
  - Programmable timing supporting DDR-1 SDRAM
  - 64-bit data interface, up to 333 MHz data rate
  - Four banks of memory supported, each up to 1 Gbyte
  - DRAM chip configurations from 64 Mbits to 1 Gbit with x8/x16 data ports
  - Full ECC support
  - Page mode support (up to 16 simultaneous open pages)
  - Contiguous or discontiguous memory mapping
  - Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
  - Sleep mode support for self refresh SDRAM
  - Supports auto refreshing
  - On-the-fly power management using CKE signal
  - Registered DIMM support
  - Fast memory access via JTAG port
  - 2.5V SSTL2 compatible I/O
- RapidIO interface unit
  - 8-bit RapidIO I/O and messaging protocols
  - Source-synchronous Double Data Rate (DDR) interfaces
  - Supports small type systems (small domain, 8-bit device ID)
  - Supports four priority levels (ordering within a level)

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- – Reordering across priority levels
- – Maximum data payload of 256 bytes per packet
- – Packet pacing support at the physical layer
- – CRC protection for packets
- – Supports atomic operations increment, decrement, set, and clear
- – LVDS signaling
- RapidIO–compliant message unit
  - – One inbound data message structure (inbox)
  - – One outbound data message structure (outbox)
  - – Supports chaining and direct modes in the outbox
  - – Support of up to 16 packets per message
  - – Support of up to 256 bytes per packet and up to 4 Kbytes of data per message
  - – Supports one inbound doorbell message structure
- Programmable Interrupt Controller (PIC)
  - – Programming model is compliant with the OpenPIC architecture
  - – Supports 16 programmable interrupt and processor task priority levels
  - – Supports 12 discrete external interrupts
  - – Supports 4 message interrupts with 32-bit messages
  - – Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
  - – Four global high resolution timers/counters that can generate interrupts
  - – Supports 22 other internal interrupt sources
  - – Supports fully nested interrupt delivery
  - – Interrupts can be routed to external pin for external processing
  - – Interrupts can be routed to the e500 core's standard or critical interrupt inputs
  - – Interrupt summary registers allow fast identification of interrupt source
- I^2C Controller
  - – Two-wire interface
  - – Multiple master support
  - – Master or slave I^2C mode support
  - – On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - – Optionally loads configuration data from serial ROM at reset via the I^2C interface
  - – Can be used to initialize configuration registers and/or memory
  - – Supports extended I^2C addressing mode
  - – Data integrity checked with preamble signature and CRC
- DUART
  - – Two 4-wire interfaces (SIN, SOUT, $\overline{RTS}$, $\overline{CTS}$)
  - – Programming model compatible with the original 16450 UART and the PC16550D
- 10/100 Fast Ethernet Controller (FEC)

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- – Operates at 10 to 100 megabits per second (Mbps) as a device debug and maintenance port
- Local Bus Controller (LBC)
    - – Multiplexed 32-bit address and data operating at up to 166 MHz
    - – Eight chip selects support eight external slaves
    - – Up to eight-beat burst transfers
    - – The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
    - – Three protocol engines available on a per chip select basis:
        - – General Purpose Chip select Machine (GPCM)
        - – Three User Programmable Machines (UPMs)
        - – Dedicated single data rate SDRAM controller
    - – Parity support
    - – Default boot ROM chip select with configurable bus width (8-,16-, or 32-bit)
- Two three-speed (10/100/1Gb) Ethernet controllers (TSECs)
    - – Dual IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab compliant controllers
    - – Support for different Ethernet physical interfaces:
        - – 10/100/1Gb Mbps IEEE 802.3 GMII
        - – 10/100 Mbps IEEE 802.3 MII
        - – 10 Mbps IEEE 802.3 MII
        - – 1000 Mbps IEEE 802.3z TBI
        - – 10/100/1Gb Mbps RGMII/RTBI
    - – Full- and half-duplex support
    - – Buffer descriptors are backward compatible with PC8260 and PC860T 10/100 programming models
    - – 9.6-Kbyte jumbo frame support
    - – RMON statistics support
    - – 2-Kbyte internal transmit and receive FIFOs
    - – MII management interface for control and status
    - – Programmable CRC generation and checking
    - – Ability to force allocation of header information and buffer descriptors into L2 cache.
- OCeaN switch fabric
    - – Four-port crossbar packet switch
    - – Reorders packets from a source based on priorities
    - – Reorders packets to bypass blocked packets
    - – Implements starvation avoidance algorithms
    - – Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
    - – Four-channel controller
    - – All channels accessible by both the local and remote masters
    - – Extended DMA functions (advanced chaining and striding capability)
    - – Support for scatter and gather transfers

- – Misaligned transfer capability
- – Interrupt on completed segment, link, list, and error
- – Supports transfers to or from any local memory or I/O port
- – Selectable hardware-enforced coherency (snoop/no-snoop)
- – Ability to start and flow control each DMA channel from external 3-pin interface
- – Ability to launch DMA from single write transaction
- PCI/PCI-X controller
  - – PCI 2.2 and PCI-X 1.0 compatible
  - – 64- or 32-bit PCI port supports at 16 to 66 MHz
  - – 64-bit PCI-X support up to 133 MHz
  - – Host and agent mode support
  - – 64-bit dual address cycle (DAC) support
  - – PCI-X supports multiple split transactions
  - – Supports PCI-to-memory and memory-to-PCI streaming
  - – Memory prefetching of PCI read accesses
  - – Supports posting of processor-to-PCI and PCI-to-memory writes
  - – PCI 3.3V compatible
  - – Selectable hardware-enforced coherency
- Power management
  - – Fully static 1.2V CMOS design with 3.3- and 2.5V I/O
  - – Supports power saving modes: doze, nap, and sleep
  - – Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle.
- System performance monitor
  - – Supports eight 32-bit counters that count the occurrence of selected events
  - – Ability to count up to 512 counter-specific events
  - – Supports 64 reference events that can be counted on any of the 8 counters
  - – Supports duration and quantity threshold counting
  - – Burstiness feature that permits counting of burst events with a programmable time between bursts
  - – Triggering and chaining capability
  - – Ability to generate an interrupt on overflow
- System access port
  - – Uses JTAG interface and a TAP controller to access entire system memory map
  - – Supports 32-bit accesses to configuration registers
  - – Supports cache-line burst accesses to main memory
  - – Supports large block (4-Kbyte) uploads and downloads
  - – Supports continuous bit streaming of entire block for fast upload and download
- IEEE 1149.1-compliant, JTAG boundary scan
- 783 HiTCE package

2. Electrical Characteristics

This section provides the electrical specifications and thermal characteristics for the PC8540. The PC8540 is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.2 Detailed Specification

This specification describes the specific requirements for the microprocessor PC8540 in compliance with e2v standard screening.

2.3 Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics
2. MIL-PRF-38535: Appendix A: General specifications for microcircuits

The microcircuits are in accordance with the applicable documents and as specified herein.

2.3.1 Absolute Maximum Ratings

Table 2-1 provides the absolute maximum ratings.

Table 2-1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage - For devices rated at 667 and 833 MHz - For devices rated at 1 GHz		V_{DD}	-0.3 to 1.32 -0.3 to 1.43	V	
PLL supply voltage - For devices rated at 667 and 833 MHz - For devices rated at 1 GHz		AV_{DD}	-0.3 to 1.32 -0.3 to 1.43	V	
DDR DRAM I/O voltage		GV_{DD}	–0.3 to 3.63	V	
Three-speed Ethernet I/O voltage		LV_{DD}	-0.3 to 3.63 -0.3 to 2.75	V	
PCI/PCI-X, local bus, RapidIO, 10/100 Ethernet, MII management, DUART, system control and power management, I^{2}C, and JTAG I/O voltage		OV_{DD}	-0.3 to 3.63	V	(3)
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	(2)(5)
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	(2)(5)
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	(4)(5)
	Local bus, RapidIO, 10/100 ethernet, DUART, SYSCLK, system control and power management, I^{2}C, and JTAG signals	OV_{IN}	-0.3 to (OV_{DD} + 0.3)	V	(5)
	PCI/PCI-X	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	(6)
Storage temperature range		T_{STG}	-55 to 150	°C	

Notes: 1. Functional and tested operating conditions are given in Table 2-2 on page 8. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

3. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

4. Caution: LV_{IN} must not exceed LV_{DD} by more than 0.3V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

5. $(M,L,O)V_{IN}$ and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2-1 on page 9.

6. OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3V operation, as shown in Figure 2-2 on page 10.

2.3.2 Power Sequencing

One consequence of multiple power supplies is that when power is initially applied the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. However, with the advancement in the PowerQUICC III ESD design, the order in which the various PowerQUICC III power rails ramp is open without adverse effect to the PowerQUICC III device as long as the supplies do not exceed to absolute maximum ratings.

2.3.3 Recommended Operating Conditions

Table 2-2 provides the recommended operating conditions for the PC8540. Note that the values in Table 2-2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

**Table 2-2.** Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit
Core supply voltage - For devices rated at 667 and 833 MHz - For devices rated at 1 GHz		V_{DD}	1.2V ± 60 mV 1.3V ± 50 mV	V
PLL supply voltage - For devices rated at 667 and 833 MHz - For devices rated at 1 GHz		AV_{DD}	1.2V ± 60 mV 1.3V ± 50 mV	V
DDR DRAM I/O voltage		GV_{DD}	2.5V ± 125 mV	V
Three-speed Ethernet I/O voltage		LV_{DD}	3.3V ± 165 mV 2.5V ± 125 mV	V
PCI/PCI-X, local bus, RapidIO, 10/100 Ethernet, MII management, DUART, system control and power management, I²C, and JTAG I/O voltage		OV_{DD}	3.3V ± 165 mV	V

Table 2-2. Recommended Operating Conditions (Continued)

Characteristic		Symbol	Recommended Value	Unit
Input voltage	DDR DRAM signals	MV_{IN}	GND to GV_{DD}	V
	DDR DRAM reference	MV_{REF}	GND to GV_{DD}	V
	Three-speed Ethernet signals	LV_{IN}	GND to LV_{DD}	V
	PCI/PCI-X, local bus, RapidIO, 10/100 Ethernet, MII management, DUART, SYSCLK, system control and power management, I²C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V
Die-junction temperature		T_J	-55/+125°C	°C

Figure 2-1 shows the undershoot and overshoot voltages at the interfaces of the PC8540.

Figure 2-1. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$
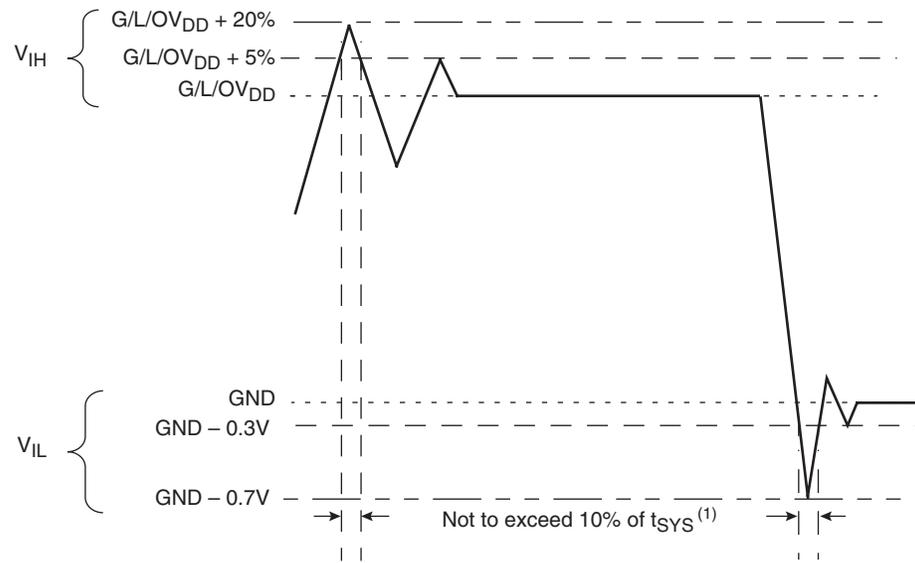

Note: 1. Note that t_{SYS} refers to the clock period associated with the SYSCLK signal.

The PC8540 core voltage must always be provided at nominal 1.2V (see Table 2-2 on page 8 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2-2 on page 8. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

Figure 2-2 shows the undershoot and overshoot voltage of the PCI interface of the PC8540 for the 3.3V signals, respectively.

Figure 2-2. Maximum AC Waveforms on PCI Interface for 3.3V Signaling
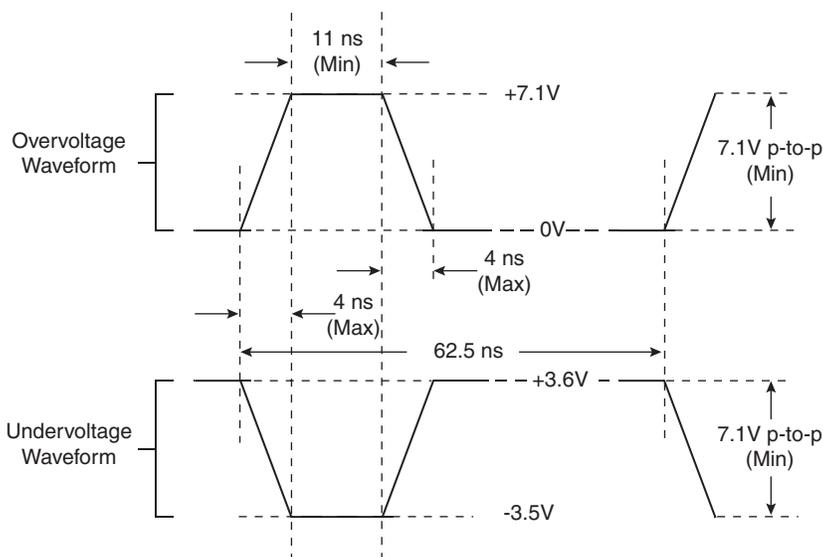
2.3.4   Output Driver Characteristics

Table 2-3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 2-3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25	OV_{DD} = 3.3V	(1)
	42 (default)		
PCI signals	25		(2)
	42 (default)		
DDR signal	20	GV_{DD} = 2.5V	
TSEC/10/100 signals	42	LV_{DD} = 2.5/3.3V	
DUART, system control, I^{2}C, JTAG	42	OV_{DD} = 3.3V	
RapidIO N/A (LVDS signaling)	N/A		

Notes: 1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.

2. The drive strength of the PCI interface is determined by the setting of the $\overline{PCI\_GNT1}$ signal at reset.

3. Power Characteristics

The estimated power dissipation on the V_{DD} supply for the PC8540 is shown in Table 3-1.

Table 3-1.   PC8540 V_{DD} Power Dissipation[1]

CCB Frequency (MHz)	Core Frequency (MHz)	Typical Power[2][3]	Maximum Power[4]	Unit
200	400	4.6	7.2	W
	500	4.9	7.5	
	600	5.3	7.9	
267	533	5.5	8.2	W
	667	5.9	8.7	
	800	6.4	10.2	
333	667	6.3	9.3	W
	833	6.9	10.9	
	1000[5]	TBD	TBD	

Notes: 1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}.

2. Typical Power is based on a nominal voltage of V_{DD} = 1.2V, a nominal process, a junction temperature of T_j = 105°C, and a Dhrystone 2.1 benchmark application.

3. Thermal solutions will likely need to design to a number higher than Typical Power based on the end application, T_A target, and I/O power.

4. Maximum power is based on a nominal voltage of V_{DD} = 1.2V, worst case process, a junction temperature of T_j = 105°C, and an artificial smoke test.

5. The nominal recommended V_{DD} is 1.3V for this speed grade.

The estimated power dissipation on the AV_{DD} supplies for the PC8540 PLLs is shown in Table 3-2.

Table 3-2.   PC8540 AV_{DD} Power Dissipation

AV_{DD}n	Typical[1]	Unit
AV_{DD}1	0.007	W
AV_{DD}2	0.014	W

Note: 1. V_{DD} = 1.2V (1.3V for 1 GHz device), T_j = 105°C.

Table 3-3 provides estimated I/O power numbers for each block: DDR, PCI, Local Bus, RapidIO, TSEC, and FEC.

Table 3-3. Estimated Typical I/O Power Consumption

Interface	Parameter	GV$_{DD}$ (2.5V)	OV$_{DD}$ (3.3V)	LV$_{DD}$ (3.3V)	LV$_{DD}$ (2.5V)	Units	Notes
DDR I/O	CCB = 200 MHz	0.46				W	[1]
	CCB = 266 MHz	0.59					
	CCB = 300 MHz	0.66					
	CCB = 333 MHz	0.73					
PCI/PCI-X I/O	32-bit, 33 MHz		0.04			W	[2]
	32-bit 66 MHz		0.07				
	64-bit, 66 MHz		0.14				
	64-bit, 133 MHz		0.25				
Local Bus I/O	32-bit, 33 MHz		0.07			W	[3]
	32-bit 66 MHz		0.13				
	32-bit, 133 MHz		0.24				
	32-bit, 167 MHz		0.30				
RapidIO I/O	500 MHz data rate		0.96			W	[4]
TSEC I/O	MII			10		mW	[5][6]
	GMII, TBI (2.5V)				40		
	GMII, TBI (3.3V)			70			
	RGMII, RTBI				40		
FEC I/O	MII		10			mW	[7]

Notes: 1. GV$_{DD}$ = 2.5, ECC enabled, 66% bus utilization, 33% write cycles, 10 pF load on data, 10 pF load on address/command, 10 pF load on clock.
2. OV$_{DD}$ = 3.3, 30 pF load per pin, 54% bus utilization, 33% write cycles.
3. OV$_{DD}$ = 3.3, 25 pF load per pin, 5 pF load on clock, 40% bus utilization, 33% write cycles.
4. V$_{DD}$ = 1.2, OV$_{DD}$ = 3.3
5. LV$_{DD}$ = 2.5/3.3, 15 pF load per pin, 25% bus utilization.
6. Power dissipation for one TSEC only.
7. OV$_{DD}$ = 3.3, 20 pF load per pin, 25% bus utilization.

4. Clock Timing

4.1 System Clock Timing

Table 4-1 provides the system clock (SYSCLK) AC timing specifications for the PC8540.

Table 4-1. SYSCLK AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	–	–	166	MHz	[1]
SYSCLK cycle time	t_{SYSCLK}	6	–	–	ns	
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1	1.2	ns	[2]
SYSCLK duty cycle	t_{KHKL}/t_{SYSCLK}	40	–	60	%	[3]
SYSCLK jitter	–	–	–	± 150	ps	[4][5]

Notes:
1. Caution: The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2 "Platform/System PLL Ratio" on page 72 and Section 15.3 "e500 Core PLL Ratio" on page 72 for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6V and 2.7V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter, short term and long term, and is guaranteed by design.
5. For spread spectrum clocking, guidelines are ± 1% of the input frequency with a maximum of 60 kHz of modulation regardless of the input frequency.

4.2 TSEC Gigabit Reference Clock Timing

Table 4-2 provides the TSEC gigabit reference clock (EC_GTX_CLK125) AC timing specifications for the PC8540.

Table 4-2. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	–	125	–	MHz	
EC_GTX_CLK125 cycle time	t_{G125}	–	8	–	ns	
EC_GTX_CLK125 rise and fall time	t_{G125R}, t_{G125F}	–	–	1	ns	[1][2]
EC_GTX_CLK125 duty cycle - GMII, TBI - RGMII, RTBI	t_{G125H}/t_{G125}	45 47	–	55 53	%	[2]

Notes:
1. Rise and fall times for EC_GTX_CLK125 are measured at 0.6V and 2.7V.
2. Timing is guaranteed by design and characterization.

4.3 RapidIO Transmit Clock Input Timing

Table 4-3 provides the RapidIO transmit clock input (RIO_TX_CLK_IN) AC timing specifications for the PC8540.

Table 4-3. RIO_TX_CLK_IN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
RIO_TX_CLK_IN frequency	f_{RCLK}	125	–	–	MHz	
RIO_TX_CLK_IN cycle time	t_{RCLK}	–	–	8	ns	
RIO_TX_CLK_IN duty cycle	t_{RCLKH}/t_{RCLK}	48	–	52	%	[1]

Note: 1. Requires ± 100 ppm long term frequency stability. Timing is guaranteed by design and characterization.

4.4 Real Time Clock Timing

Table 4-4 provides the Real Time Clock (RTC) AC timing specifications for the PC8540.

Table 4-4. RTC AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
RTC clock high time	t_{RTCH}	$2 \times t_{CCB\_CLK}$	–	–	ns	
RTC clock low time	t_{RTCL}	$2 \times t_{CCB\_CLK}$	–	–	ns	

5. Reset Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the PC8540. Table 5-1 provides the RESET initialization AC timing specifications for the PC8540.

Table 5-1. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{HRESET}$	100	–	µs	
Minimum assertion time for $\overline{SRESET}$	512	–	SYSCLKs	[1]
PLL input setup time with stable SYSCLK before $\overline{HRESET}$ negation	100	–	µs	
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{HRESET}$	4	–	SYSCLKs	[1]
Input hold time for POR configs (including PLL config) with respect to negation of $\overline{HRESET}$	2	–	SYSCLKs	[1]
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{HRESET}$	–	5	SYSCLKs	[1]

Note: 1. SYSCLK is identical to the PCI_CLK signal and is the primary clock input for the PC8540. See the PC8540 Integrated Processor Preliminary Reference Manual for more details.

Table 5-2 provides the PLL and DLL lock times.

Table 5-2. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	–	100	µs	
DLL lock times	7680	122,880	CCB Clocks	[1][2]

Notes: 1. DLL lock times are a function of the ratio between the output clock and the platform (or CCB) clock. A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The CCB clock is determined by the SYSCLK × platform PLL ratio.

6. DDR SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the PC8540.

6.1 DDR SDRAM DC Electrical Characteristics

Table 6-1 provides the recommended operating conditions for the DDR SDRAM component(s) of the PC8540.

Table 6-1. DDR SDRAM DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	[1]
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	[2]
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	[3]
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	[4]
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.18$	V	[4]
Output leakage current	I_{OZ}	-10	10	µA	[5]
Output high current (V_{OUT} = 1.95V)	I_{OH}	-15.2	–	mA	
Output low current (V_{OUT} = 0.35V)	I_{OL}	15.2	–	mA	
MV_{REF} input leakage current	IV_{REF}	–	5	µA	

Notes: 1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GVDDDC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ± 2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. V_{IH} can tolerate an overshoot of 1.2V over GV_{DD} for a pulse width of ≤ 3 ns, and the pulse width cannot be greater than t_{MCK}. V_{IL} can tolerate an undershoot of 1.2V below GND for a pulse width of ≤ 3 ns, and the pulse width cannot be greater than t_{MCK}.
5. Output leakage is measured with all outputs disabled, $0V \leq V_{OUT} \leq GV_{DD}$.

Table 6-2 provides the DDR capacitance.

Table 6-2. DDR SDRAM Capacitance

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, MSYNC_IN	C_{IO}	6	8	pF	[1]
Delta input/output capacitance: DQ, DQS	C_{DIO}	–	0.5	pF	[1]

Note: 1. This parameter is sampled. $GV_{DD} = 2.5V \pm 0.125V$, f = 1 MHz, $T_A = 25°C$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2V.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 6-3 provides the input AC timing specifications for the DDR SDRAM interface.

Table 6-3. DDR SDRAM Input AC Timing Specifications (At Recommended Operating Conditions with GV_{DD} of 2.5V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	–	MV_{REF} -0.31	V	
AC input high voltage	V_{IH}	MV_{REF} + 0.31	GV_{DD} + 0.3	V	
MDQS–MDQ/MECC input skew per byte - For DDR = 333 MHz - For DDR ≤ 266 MHz	t_{DISKEW}	-750 -1125	750 1125	ps	[1][2]

Notes: 1. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 ≤ n ≤ 7) or ECC (MECC[{0...7}] if n = 8).

2. For timing budget analysis, the PC8540 consumes ± 550 ps of the total budget.

Figure 6-1. DDR SDRAM Interface Input Timing
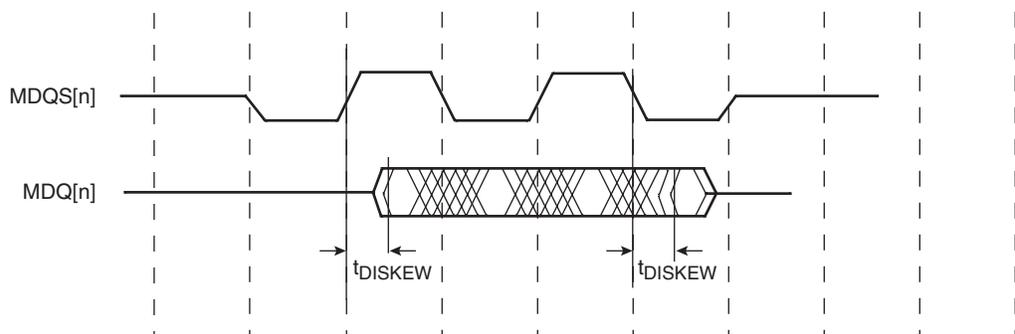
6.2.2 DDR SDRAM Output AC Timing Specifications

For chip selects $\overline{MCS1}$ and $\overline{MCS2}$, there will always be at least 200 DDR memory clocks coming out of self-refresh after an $\overline{HRESET}$ before a precharge occurs. This will not necessarily be the case for chip selects $\overline{MCS0}$ and $\overline{MCS3}$.

6.2.2.1 DLL Enabled Mode

Table 6-4 and Table 6-5 on page 18 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface with the DDR DLL enabled.

Table 6-4. DDR SDRAM Output AC Timing Specifications - DLL Mode (At Recommended Operating Conditions with GV_{DD} of 2.5V ± 5%)

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/$\overline{MCK}$[n] crossing)	t_{MCK}	6	10	ns	[2]
On chip Clock Skew	$t_{MCKSKEW}$	–	150	ps	[3][8]
MCK[n] duty cycle	t_{MCKH}/t_{MCK}	45	55	%	[8]
ADDR/CMD output valid	t_{DDKHOV}	–	3	ns	[4][9]
ADDR/CMD output invalid	t_{DDKHOX}	1	–	ns	[4][9]
Write CMD to first MDQS capture edge	t_{DDSHMH}	t_{MCK} + 1.5	t_{MCK} + 4	ns	[5]
MDQ/MECC/MDM output setup with respect to MDQS - 333 MHz - 266 MHz - 200 MHz	t_{DDKHDS}, t_{DDKLDS}	900 1100 1200	–	ps	[6][9]
MDQ/MECC/MDM output hold with respect to MDQS - 333 MHz - 266 MHz - 200 MHz	t_{DDKHDX}, t_{DDKLDX}	900 1100 1200	–	ps	[6][9]
MDQS preamble start	t_{DDSHMP}	$0.75 \times t_{MCK}$ + 1.5	$0.75 \times t_{MCK}$ + 4	ns	[7][8]
MDQS epilogue end	t_{DDSHME}	1.5	4	ns	[7][8]

Notes: 1. The symbols used for timing specifications follow the pattern of t(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t(first two letters of functional block)(reference)(state)(signal)(state) for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (OX or DX). For example, t_{DDKHOV} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (O) are valid (V) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.

2. All MCK/$\overline{MCK}$ referenced measurements are made from the crossing of the two signals ± 0.1V.

3. Maximum possible clock skew between a clock MCK[n] and its relative inverse clock $\overline{MCK}$[n], or between a clock MCK[n] and a relative clock MCK[m] or MSYNC_OUT. Skew measured between complementary signals at GV_{DD}/2.

4. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{MCK}$ and MDQ/MECC/MDM/MDQS.

5. Note that t_{DDSHMH} follows the symbol conventions described in note 1. For example, t_{DDSHMH} describes the DDR timing (DD) from the rising edge of the MSYNC_IN clock (SH) until the MDQS signal is valid (MH). t_{DDSHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. These controls allow the relationship between the synchronous clock control timing and the source-synchronous DQS domain to be modified by the user. For best turnaround times, these may need to be set to delay t_{DDSHMH} an additional 0.25t_{MCK}. This will also affect t_{DDSHMP} and t_{DDSHME} accordingly. See the PC8540 Integrated Processor Preliminary Reference Manual for a description and understanding of the timing modifications enabled by use of these bits.

6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the PC8540.

7. All outputs are referenced to the rising edge of MSYNC_IN (S) at the pins of the PC8540. Note that t_{DDSHMP} follows the symbol conventions described in note 1. For example, t_{DDSHMP} describes the DDR timing (DD) from the rising edge of the MSYNC_IN clock (SH) for the duration of the MDQS signal precharge period (MP).

8. Guaranteed by design.

9. Guaranteed by characterization.

Figure 6-2 provides the AC test load for the DDR bus.

Figure 6-2. DDR AC Test Load

Table 6-5. DDR SDRAM Measurement Conditions

Symbol	DDR	Unit	Notes
V_{TH}	$MV_{REF} \pm 0.31V$	V	[1]
V_{OUT}	$0.5 \times GV_{DD}$	V	[2]

Notes: 1. Data input threshold measurement point.
2. Data output measurement point.

Figure 6-3 shows the DDR SDRAM output timing diagram.

Figure 6-3. DDR SDRAM Output Timing Diagram

6.2.2.2   *Load Effects on Address/Command Bus*

Table 6-6 on page 19 provides approximate delay information that can be expected for the address and command signals of the DDR controller for various loadings. These numbers are the result of simulations for one topology. The delay numbers will strongly depend on the topology used. These delay numbers show the total delay for the address and command to arrive at the DRAM devices. The actual delay could be different than the delays seen in simulation, depending on the system topology. If a heavily loaded system is used, the DLL loop may need to be adjusted to meet setup requirements at the DRAM.

Table 6-6. Expected Delays for Address/Command

Load	Delay	Unit
4 devices (12 pF)	3	ns
9 devices (27 pF)	3.6	ns
36 devices (108 pF) + 40 pF compensation capacitor	5	ns
36 devices (108 pF) + 80 pF compensation capacitor	5.2	ns

7. DUART

This section describes the DC and AC electrical specifications for the DUART interface of the PC8540.

7.1 DUART DC Electrical Characteristics

Table 7-1 provides the DC electrical characteristics for the DUART interface of the PC8540.

Table 7-1. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current (V_{IN}[1] = 0V or $V_{IN} = V_{DD}$)	I_{IN}	–	± 5	µA
High-level output voltage (OV_{DD} = min, I_{OH} = -100 µA)	V_{OH}	$OV_{DD} - 0.2$	–	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 µA)	V_{OL}	–	0.2	V

Note: 1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2-1 on page 7 and Table 2-2 on page 8.

7.2 DUART AC Electrical Specifications

Table 7-2 provides the AC timing parameters for the DUART interface of the PC8540.

Table 7-2. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	$f_{CCB\_CLK}/1048576$	baud	[3]
Maximum baud rate	$f_{CCB\_CLK}/16$	baud	[1][3]
Oversample rate	16	–	[2][3]

Notes: 1. Actual attainable baud rate will be limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.
3. Guaranteed by design.

8. Ethernet: Three-Speed,10/100, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100, and MII management.

8.1 Three-Speed Ethernet Controller (TSEC) (10/100/1Gb Mbps)–GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), MII (Media Independent Interface), TBI (Ten-Bit Interface), RGMII (Reduced Gigabit Media Independent Interface), and RTBI (Reduced Ten-Bit Interface) signals except MDIO (Management Data Input/Output) and MDC (Management Data Clock). The RGMII and RTBI interfaces are defined for 2.5V, while the GMII, MII, and TBI interfaces can be operated at 3.3 or 2.5V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5V, the timing is compliant with the IEEE 802.3 standard. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.4 "Ethernet Management Interface Electrical Characteristics" on page 31.

8.1.1 TSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 8-1 and Table 8-2 on page 21. The potential applied to the input of a GMII, MII, TBI, RGMII, or RTBI receiver may exceed the potential of the receiver's power supply (i.e., a GMII driver powered from a 3.6V supply driving V_{OH} into a GMII receiver powered from a 2.5V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 8-1. GMII, MII, and TBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3V	LV_{DD}	3.13	3.47	V
Output high voltage (LV_{DD} = Min, I_{OH} = -4 mA)	V_{OH}	2.40	LV_{DD} + 0.3	V
Output low voltage (LV_{DD} = Min, I_{OL} = 4 mA)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	1.70	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	-0.3	0.90	V
Input high current (V_{IN}[1] = LV_{DD})	I_{IH}	–	40	µA
Input low current (V_{IN}[1] = GND)	I_{IL}	-600	–	µA

Note: 1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2-1 on page 7 and Table 2-2 on page 8.

Table 8-2. GMII, MII, RGMII, RTBI, and TBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage 2.5V	LV_{DD}	2.37	2.63	V
Output high voltage (LV_{DD} = Min, I_{OH} = -1 mA)	V_{OH}	2	LV_{DD} + 0.3	V
Output low voltage (LV_{DD} = Min, I_{OL} = 1 mA)	V_{OL}	GND – 0.3	0.40	V
Input high voltage	V_{IH}	1.70	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	-0.3	0.70	V
Input high current (V_{IN}[1] = LV_{DD})	I_{IH}	–	10	µA
Input low current (V_{IN}[1] = GND)	I_{IL}	-15	–	µA

Note: 1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2-1 on page 7 and Table 2-2 on page 82.

8.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.1.1 GMII Transmit AC Timing Specifications

Table 8-3 provides the GMII transmit AC timing specifications.

Table 8-3. GMII Transmit AC Timing Specifications (At Recommended Operating Conditions with LV_{DD} of 3.3V ± 5%)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{GTX}	–	8	–	ns
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	40	–	60	%
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	–	–	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}[3]	0.5	–	5	ns
GTX_CLK data clock rise and fall time	t_{GTXR}, t_{GTXF}[2][4]	–	–	1	ns

Notes: 1. The symbols used for timing specifications herein follow the pattern t(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (Rise) or F (Fall).

2. Signal timings are measured at 0.7V and 1.9V voltage levels.

3. Guaranteed by characterization.

4. Guaranteed by design.

Figure 8-1 shows the GMII transmit AC timing diagram

Figure 8-1. GMII Transmit AC Timing Diagram
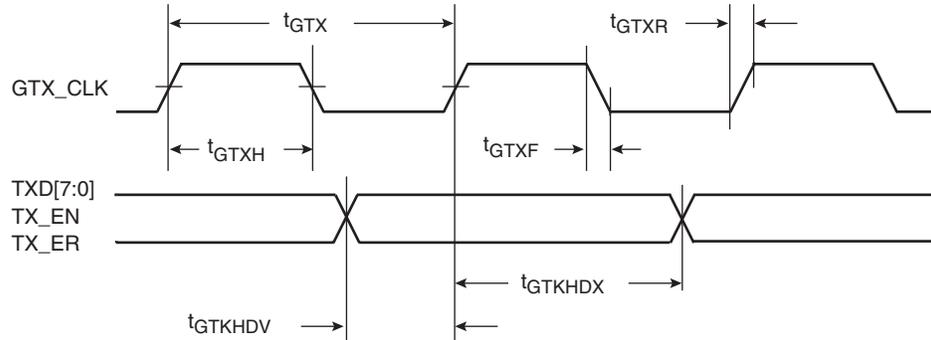
8.2.1.2 GMII Receive AC Timing Specifications

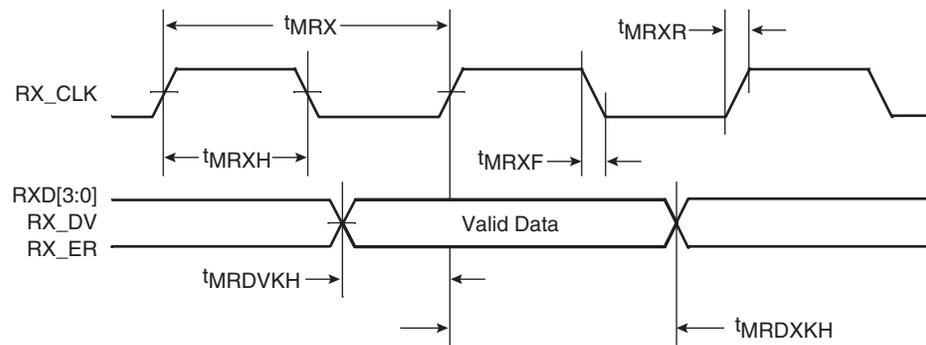Table 8-4 provides the GMII receive AC timing specifications.

Table 8-4. GMII Receive AC Timing Specifications (At Recommended Operating Conditions with LV_{DD} of 3.3V ± 5%)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	–	8	–	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	–	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2	–	–	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	–	–	ns
RX_CLK clock rise and fall time	t_{GRXR}, t_{GRXF}[2][3]	–	–	1	ns

Notes: 1. The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block)(signal)(state) (reference)(state)}}$for inputs and $t_{(\text{first two letters of functional block)(reference)(state)(signal)(state)}}$for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7V and 1.9V voltage levels.
3. Guaranteed by design.

Figure 8-2 provides the AC test load for TSEC.

Figure 8-2. TSEC AC Test Load
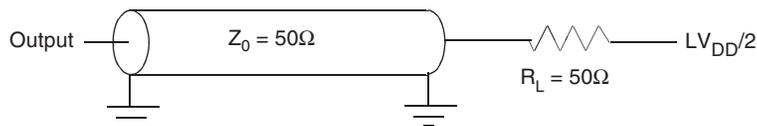
Figure 8-3 shows the GMII receive AC timing diagram.

Figure 8-3. GMII Receive AC Timing Diagram
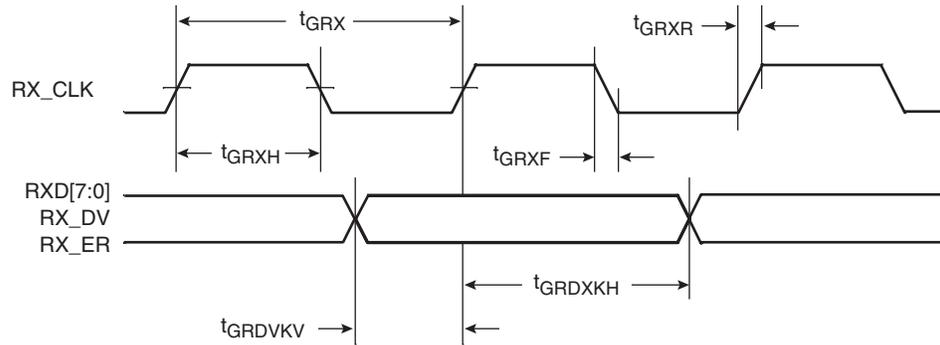
8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

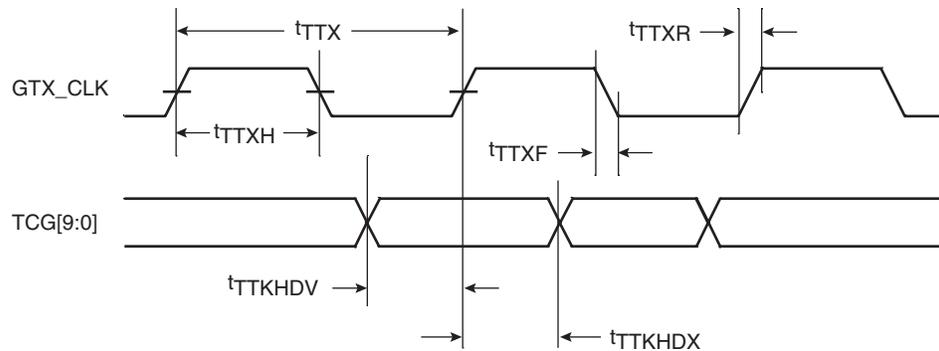Table 8-5 provides the MII transmit AC timing specifications.

Table 8-5. MII Transmit AC Timing Specifications (At Recommended Operating Conditions with LV_{DD} of 3.3V ± 5%)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}[2]		400		ns
TX_CLK clock period 100 Mbps	t_{MTXH}/t_{MTX}		40		ns
TX_CLK duty cycle	t_{MTX}	35		65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise and fall time	t_{MTXR}, t_{MTXF}[2][3]	1		4	ns

Notes: 1. The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. Signal timings are measured at 0.7V and 1.9V voltage levels.

3. Guaranteed by design.

Figure 8-4 shows the MII transmit AC timing diagram.

Figure 8-4. MII Transmit AC Timing Diagram
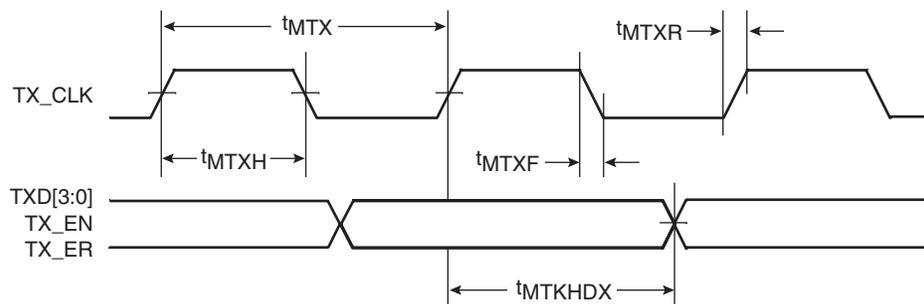
8.2.2.2   MII Receive AC Timing Specifications

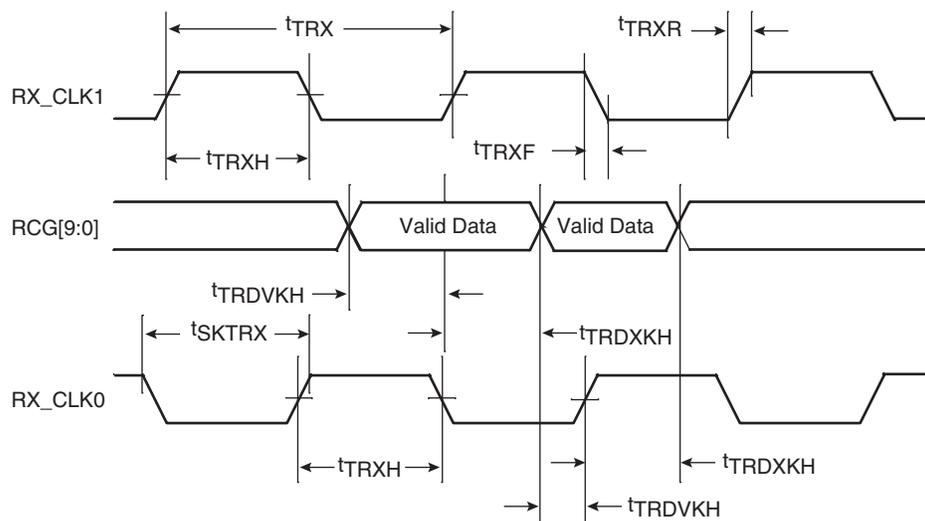Table 8-6 provides the MII receive AC timing specifications.

Table 8-6.   MII Receive AC Timing Specifications (At Recommended Operating Conditions with LV$_{DD}$ of 3.3V ± 5%)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}[3]	–	400	–	ns
RX_CLK clock period 100 Mbps	t_{MRX}	–	40	–	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	–	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10	–	–	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10	–	–	ns
RX_CLK clock rise and fall time	t_{MRXR}, t_{MRXF}[2][3]	1	–	4	ns

Notes: 1. The symbols used for timing specifications herein follow the pattern of t(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. Signal timings are measured at 0.7V and 1.9V voltage levels.

3. Guaranteed by design.

Figure 8-5 shows the MII receive AC timing diagram.

Figure 8-5.   MII Receive AC Timing Diagram

8.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.3.1 TBI Transmit AC Timing Specifications

Table 8-7 provides the TBI transmit AC timing specifications.

Table 8-7. Transmit AC Timing Specifications (At Recommended Operating Conditions with LV_{DD} of 3.3V ± 5%)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	–	8	–	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	–	60	%
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2	–	–	ns
TCG[9:0] hold time from GTX_CLK going high	t_{TTKHDX}	1	–	–	ns
GTX_CLK clock rise and fall time	t_{TTXR}, t_{TTXF}[2][3]	–	–	1	ns

Note: 1. The symbols used for timing specifications herein follow the pattern of t(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. Signal timings are measured at 0.7V and 1.9V voltage levels.

3. Guaranteed by design.

Figure 8-6 shows the TBI transmit AC timing diagram.

Figure 8-6. TBI Transmit AC Timing Diagram

8.2.3.2   TBI Receive AC Timing Specifications

Table 8-8 provides the TBI receive AC timing specifications.

**Table 8-8.**   TBI Receive AC Timing Specifications (At Recommended Operating Conditions with LV_{DD} of 3.3V ± 5%)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRX}	–	16	–	ns
RX_CLK skew	t_{SKTRX}	7.5	–	8.5	ns
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	–	60	%
RCG[9:0] setup time to rising RX_CLK	t_{TRDVKH}	2.5	–	–	ns
RCG[9:0] hold time to rising RX_CLK	t_{TRDXKH}	1.5	–	–	ns
RX_CLK clock rise time and fall time	t_{TRXR}, t_{TRXF}[2][3]	0.7	–	2.4	ns

Notes: 1. The symbols used for timing specifications herein follow the pattern of t(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).

2. Signal timings are measured at 0.7V and 1.9V voltage levels.

3. Guaranteed by design.

Figure 8-7 shows the TBI receive AC timing diagram.

Figure 8-7.   TBI Receive AC Timing Diagram

8.2.4 RGMII and RTBI AC Timing Specifications

Table 8-9 presents the RGMII and RTBI AC timing specifications.

Table 8-9. RGMII and RTBI AC Timing Specifications (At Recommended Operating Conditions with LV_{DD} of 2.5V ± 5%)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}[5]	-500	0	500	ps
Data to clock input skew (at receiver)[2]	$t_{SKRG}T$	1	–	2.8	ns
Clock cycle duration[3]	t_{RGT}[6]	7.2	8	8.8	ns
Duty cycle for 1000Base-T[4]	t_{RGTH}/t_{RGT}[6]	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX[3]	t_{RGTH}/t_{RGT}[6]	40	50	60	%
Rise and fall time	t_{RGTR}, t_{RGTF}[6][7]	–	–	0.75	ns

Notes: 1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).

2. The RGMII specification requires that PC board designer add 1.5 ns or greater in trace delay to the RX_CLK in order to meet this specification. However, as stated above, this device will function with only 1 ns of delay.

3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.

4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.

5. Guaranteed by characterization.

6. Guaranteed by design.

7. Signal timings are measured at 0.5V and 2V voltage levels.

Figure 8-8 shows the RGMII and RTBI AC timing and multiplexing diagrams.

Figure 8-8.   RGMII and RTBI AC Timing and Multiplexing Diagrams
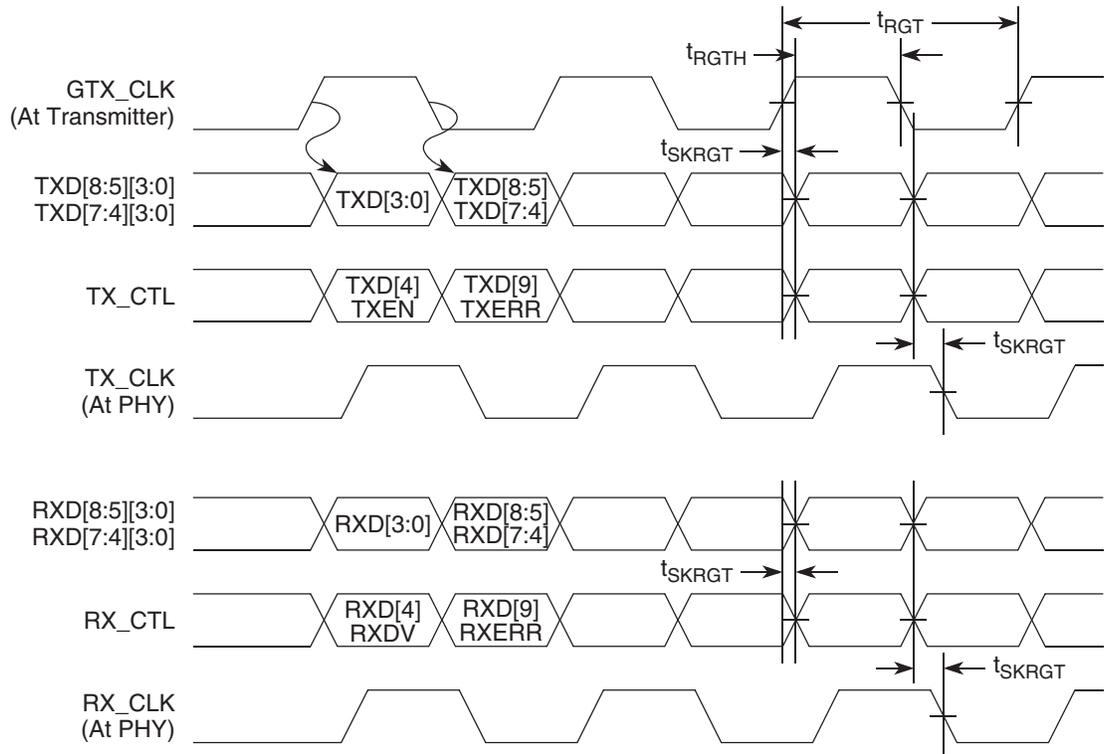
8.3   10/100 Ethernet Controller (10/100 Mbps)–MII Electrical Characteristics

The electrical characteristics specified here apply to the MII (media independent interface) signals except MDIO (management data input/output) and MDC (management data clock). The MII interface can be operated at 3.3 or 2.5V. Whether the MII interface is operated at 3.3 or 2.5V, the timing is compliant with the IEEE 802.3 standard. The electrical characteristics for MDIO and MDC are specified in Section 2.3.3 "Recommended Operating Conditions" on page 8.

8.3.1   MII DC Electrical Characteristics

All MII drivers and receivers comply with the DC parametric attributes specified in Table 8-10 on page 29. The potential applied to the input of a MII receiver may exceed the potential of the receiver's power supply (that is, a MII driver powered from a 3.6V supply driving V_{OH} into a MII receiver powered from a 2.5V supply). Tolerance for dissimilar MII driver and receiver supply potentials is implicit in these specifications.

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Table 8-10. MII DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3V	**OV_{DD}**	**3.13**	**3.47**	**V**
Output high voltage (OV_{DD} = Min, I_{OH} = -4 mA)	**V_{OH}**	**2.40**	**OV_{DD} + 0.3**	**V**
Output low voltage (OV_{DD} = Min, I_{OL} = 4 mA)	V_{OL}	GND	0.50	V
Input high voltage	**V_{IH}**	**1.70**	**–**	**V**
Input low voltage	V_{IL}	-0.3	0.90	V
Input high current (V_{IN} = OV_{DD}[1])	IIH	–	40	µA
Input low current (V_{IN} = GND[1])	IIL	-600	–	µA

Note: 1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2-1 on page 7 and Table 2-2 on page 8.

8.3.2 MII AC Electrical Specifications

This section describes the MII transmit and receive AC specifications.

8.3.2.1 MII Transmit AC Timing Specifications

Table 8-11 provides the MII transmit AC timing specifications.

Table 8-11. MII Transmit AC Timing Specifications (At Recommended Operating Conditions with OV_{DD} of 3.3V ± 5%)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	–	400	–	ns
TX_CLK clock period 100 Mbps	t_{MTX}	–	40	–	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	–	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise and fall time	t_{MTXR}, t_{MTXF}[2][3]	1	–	4	ns

Notes: 1. The symbols used for timing specifications herein follow the pattern of t(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) from the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII (M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Signal timings are measured at 0.7V and 1.9V voltage levels.
3. Guaranteed by design.

Figure 8-9 shows the MII transmit AC timing diagram.

Figure 8-9. MII Transmit AC Timing Diagram
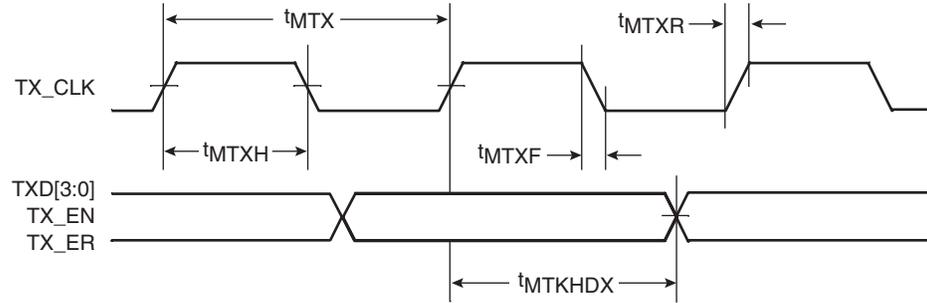
8.3.2.2 MII Receive AC Timing Specifications

Table 8-12 provides the MII receive AC timing specifications.

**Table 8-12.** MII Receive AC Timing Specifications

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	–	400	–	ns
RX_CLK clock period 100 Mbps	t_{MRX}	–	40	–	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	–	65	%
RXD[7:0], TX_DV, TX_ER setup time to RX_CLK	t_{MRDVKH}	10	–	–	ns
RXD[7:0], TX_DV, TX_ER hold time to RX_CLK	t_{MRDXKH}	10	–	–	ns
RX_CLK clock rise and fall time	t_{MRXR}, t_{MRXF}[2][3]	1	–	4	ns

Notes: 1. The symbols used for timing specifications herein follow the pattern of t(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKH} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the high (H) state or hold time. Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. Signal timings are measured at 0.7V and 1.9V voltage levels.

3. Guaranteed by design.

Figure 8-10 shows the MII receive AC timing diagram.

Figure 8-10. MII Receive AC Timing Diagram
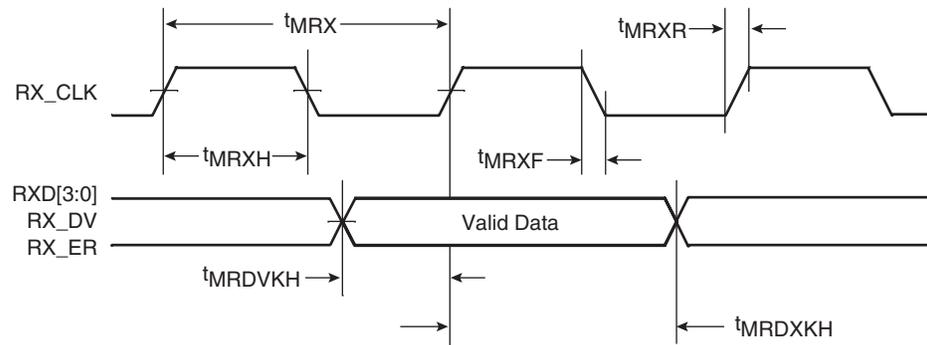
8.4 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 8.1 "Three-Speed Ethernet Controller (TSEC) (10/100/1Gb Mbps)–GMII/MII/TBI/RGMII/RTBI Electrical Characteristics" on page 20.

8.4.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3V. The DC electrical characteristics for MDIO and MDC are provided in Table 8-13.

Table 8-13. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3V)	OV_{DD}	3.13	3.47	V
Output high voltage (OV_{DD} = Min, I_{OH} = -1 mA)	V_{OH}	2.10	OV_{DD} + 0.3	V
Output low voltage (OV_{DD} = Min, I_{OL} = 1 mA)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	1.70	–	V
Input low voltage	V_{IL}	–	0.90	V
Input high current (OV_{DD} = Max, V_{IN}[1] = 2.1V)	I_{IH}	–	40	µA
Input low current (OV_{DD} = Max, V_{IN} = 0.5V)	I_{IL}	-600	–	µA

Note: 1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2-1 on page 7 and Table 2-2 on page 8.

8.4.2 MII Management AC Electrical Specifications

Table 8-14 provides the MII management AC timing specifications.

Table 8-14. MII Management AC Timing Specifications (At Recommended Operating Conditions with OV_{DD} is 3.3V ± 5%)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	0.893	–	10.4	MHz	[2][4]
MDC period	t_{MDC}	96	–	1120	ns	
MDC clock pulse width high	t_{MDCH}	32	–	–	ns	
MDC to MDIO valid	t_{MDKHDV}	–	–	$2*[1/(f_{ccb\_clk}/8)]$	ns	[3]
MDC to MDIO delay	t_{MDKHDX}	10	–	$2*[1/(f_{ccb\_clk}/8)]$	ns	[3]
MDIO to MDC setup time	t_{MDDVKH}	5	–	–	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	–	–	ns	
MDC rise time	t_{MDCR}	–	–	10	ns	[4]
MDC fall time	t_{MDHF}	–	–	10	ns	[4]

Notes: 1. The symbols used for timing specifications herein follow the pattern of t$_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and t$_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t$_{\text{MDKHDX}}$ symbolizes management data timing (MD) for the time t$_{\text{MDC}}$ from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t$_{\text{MDDVKH}}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t$_{\text{MDC}}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. This parameter is dependent on the CCB clock speed (that is, for a CCB clock of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a CCB clock of 333 MHz, the maximum frequency is 10.4 MHz and the minimum frequency is 1.5 MHz).

3. This parameter is dependent on the CCB clock speed (that is, for a CCB clock of 267 MHz, the delay is 60 ns and for a CCB clock of 333 MHz, the delay is 48 ns).

4. Guaranteed by design.

Figure 8-11 shows the MII management AC timing diagram.

Figure 8-11. MII Management Interface Timing Diagram
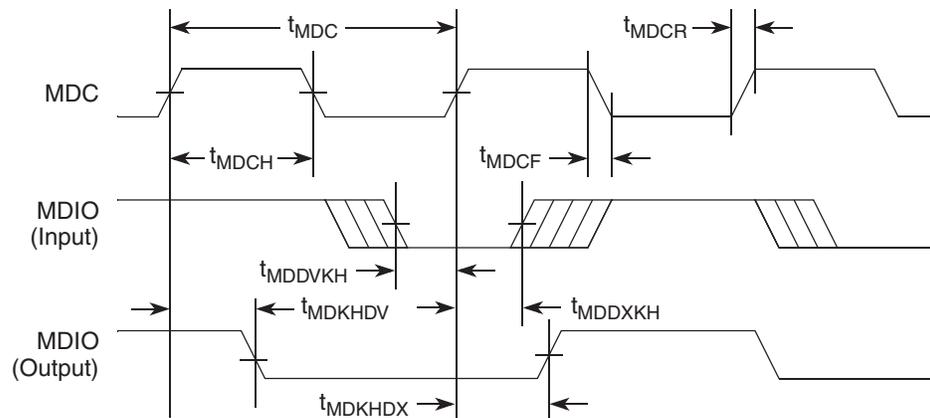
9. Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the PC8540.

9.1 Local Bus DC Electrical Characteristics

Table 9-1 provides the DC electrical characteristics for the local bus interface.

Table 9-1.   Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current ($V_{IN}^{(1)}$ = 0 V or $V_{IN} = V_{DD}$)	I_{IN}	–	± 5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	OV_{DD} - 0.2	–	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	–	0.2	V

Note: 1.   Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2-1 on page 7 and Table 2-2 on page 8.

9.2 Local Bus AC Electrical Specifications

Table 9-2 describes the general timing parameters of the local bus interface of the PC8540 with the DLL enabled.

Table 9-2. Local Bus General Timing Parameters - DLL Enabled

Parameter	POR Configuration	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time		t_{LBK}	6		ns	[2]
LCLK[n] skew to LCLK[m] or LSYNC_OUT		$t_{LBKSKEW}$		150	ps	[3][9]
Input setup to local bus clock (except LUPWAIT)		$t_{LBIVKH1}$	1.8		ns	[4][5][8]
LUPWAIT input setup to local bus clock		$t_{LBIVKH2}$	1.7		ns	[4][5]
Input hold from local bus clock (except LUPWAIT)		$t_{LBIXKH1}$	0.5		ns	[4][5][8]
LUPWAIT input hold from local bus clock		$t_{LBIXKH2}$	1		ns	[4][5]
LALE output transition to LAD/LDP output transition (LATCH hold time)		t_{LBOTOT}	1.5		ns	[6]
Local bus clock to output valid (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKHOV1}$		2	ns	[8]
	TSEC2_TXD[6:5] = 11 (default)			3.5		
Local bus clock to data valid for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKHOV2}$		2.2	ns	[4][8]
	TSEC2_TXD[6:5] = 11 (default)			3.7		
Local bus clock to address valid for LAD, and LALE	TSEC2_TXD[6:5] = 00	$t_{LBKHOV3}$		2.3	ns	[4][8]
	TSEC2_TXD[6:5] = 11 (default)			3.8		
Output hold from local bus clock (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKHOX1}$	0.7		ns	[4][8]
	TSEC2_TXD[6:5] = 11 (default)	1.6			
Output hold from local bus clock for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKHOX2}$	0.7		ns	[4][8]
	TSEC2_TXD[6:5] = 11 (default)	1.6			
Local bus clock to output high Impedance (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKHOZ1}$		2.5	ns	[7][9]
	TSEC2_TXD[6:5] = 11 (default)			3.8		
Local bus clock to output high impedance for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKHOZ2}$		2.5	ns	[7][9]
	TSEC2_TXD[6:5] = 11 (default)			3.8		

Notes: 1. The symbols used for timing specifications herein follow the pattern of t(First two letters of functional block)(signal)(state) (reference)(state) for inputs and t(First two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

2. All timings are in reference to LSYNC_IN for DLL enabled mode.

3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $OV_{DD}/2$.

4. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN for DLL enabled to $0.4 \times OV_{DD}$ of the signal in question for 3.3V signaling levels.

5. Input timings are measured at the pin.

6. The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins TSEC2_TXD[6:5].

7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

8. Guaranteed by characterization.

9. Guaranteed by design.

Table 9-3 describes the general timing parameters of the local bus interface of the PC8540 with the DLL bypassed.

Table 9-3. Local Bus General Timing Parameters - DLL Enabled

Parameter	POR Configuration	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time		t_{LBK}	6	–	ns	[2]
Internal launch/capture clock to LCLK delay		t_{LBKHKT}	2.3	3.9	ns	[8]
LCLK[n] skew to LCLK[m] or LSYNC_OUT		$t_{LBKSKEW}$	–	150	ps	[3][9]
Input setup to local bus clock (except LUPWAIT)		$t_{LBIVKH1}$	5.7	–	ns	[4][5]
LUPWAIT input setup to local bus clock		$t_{LBIVKH2}$	5.6	–	ns	[4][5]
Input hold from local bus clock (except LUPWAIT)		$t_{LBIXKH1}$	-1.8	–		[4][5]
LUPWAIT input hold from local bus clock		$t_{LBIXKH2}$	-1.3	–		[4][5]
LALE output transition to LAD/LDP output transition (LATCH hold time)		t_{LBOTOT}	1.5	–		[6]
Local bus clock to output valid (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKLOV1}$	–	-0.3	ns	
	TSEC2_TXD[6:5] = 11 (default)			1.2		
Local bus clock to data valid for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKLOV2}$	–	-0.1	ns	[4]
	TSEC2_TXD[6:5] = 11 (default)			1.4		
Local bus clock to address valid for LAD, and LALE	TSEC2_TXD[6:5] = 00	$t_{LBKLOV3}$	–	0	ns	[4]
	TSEC2_TXD[6:5] = 11 (default)			1.5		
Output hold from local bus clock (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKLOX1}$	-3.2	–	ns	[4]
	TSEC2_TXD[6:5] = 11 (default)		-2.3			

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Table 9-3. Local Bus General Timing Parameters - DLL Enabled (Continued)

Parameter	POR Configuration	Symbol[1]	Min	Max	Unit	Notes
Output hold from local bus clock for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKLOX2}$	-3.2	–	ns	[4]
	TSEC2_TXD[6:5] = 11 (default)		-2.3			
Local bus clock to output high Impedance (except LAD/LDP and LALE)	TSEC2_TXD[6:5] = 00	$t_{LBKLOZ1}$	–	0.2	ns	[7]
	TSEC2_TXD[6:5] = 11 (default)			1.5		
Local bus clock to output high impedance for LAD/LDP	TSEC2_TXD[6:5] = 00	$t_{LBKLOZ2}$		0.2	ns	[7]
	0.2ns7TSEC2_TXD[6:5] = 11 (default)			1.5		

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{(First\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(First\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

2. All timings are in reference to local bus clock for DLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which preceeds LCLK by t_{LBKHKT}.

3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $OV_{DD}/2$.

4. All signals are measured from $OV_{DD}/2$ of the rising edge of local bus clock for DLL bypass mode to $0.4 \times OV_{DD}$ of the signal in question for 3.3V signaling levels.

5. Input timings are measured at the pin.

6. The value of t_{LBOTOT} is defined as the sum of 1/2 or 1 ccb_clk cycle as programmed by LBCR[AHD], and the number of local bus buffer delays used as programmed at power-on reset with configuration pins TSEC2_TXD[6:5].

7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

8. Guaranteed by characterization.

9. Guaranteed by design.

Figure 9-1 provides the AC test load for the local bus.

Figure 9-1. Local Bus AC Test Load
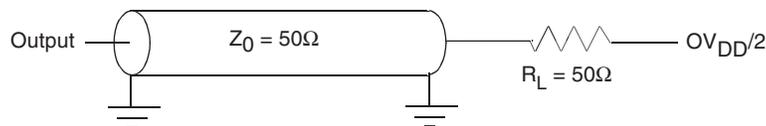
Figure 9-2. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)
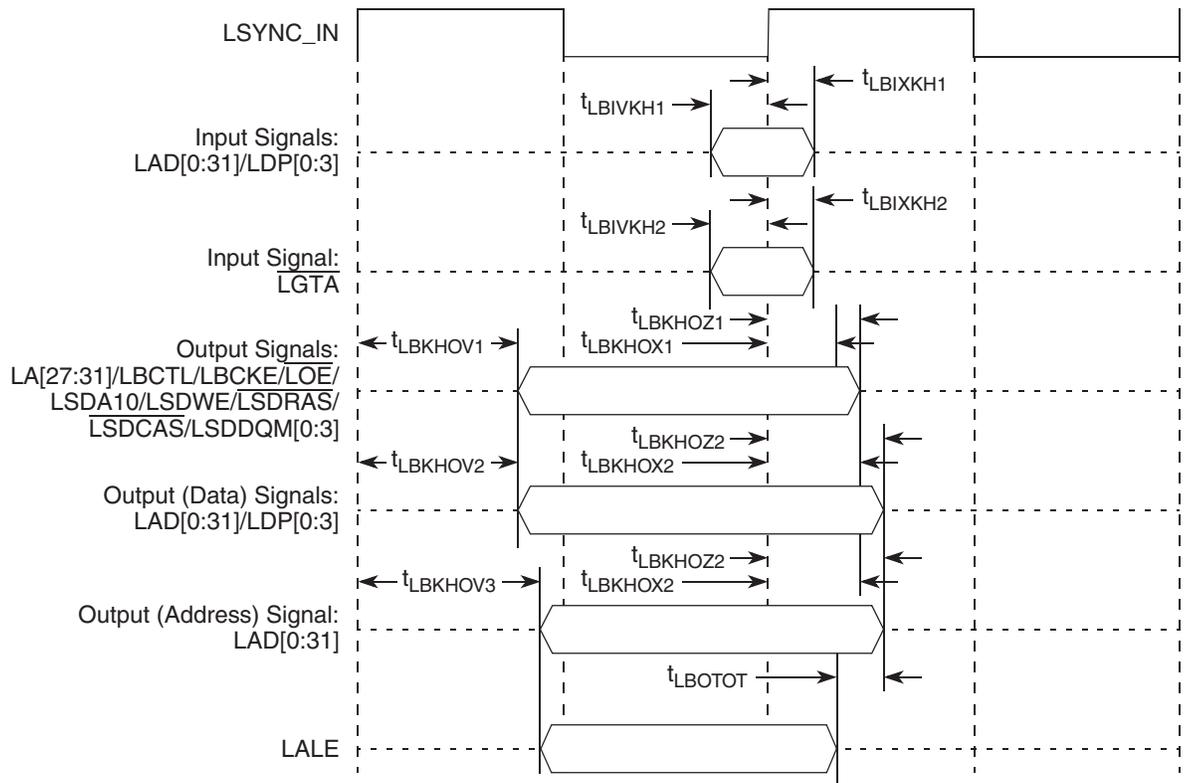
Figure 9-3. Local Bus Signals (DLL Bypass Mode)

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Figure 9-4. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)
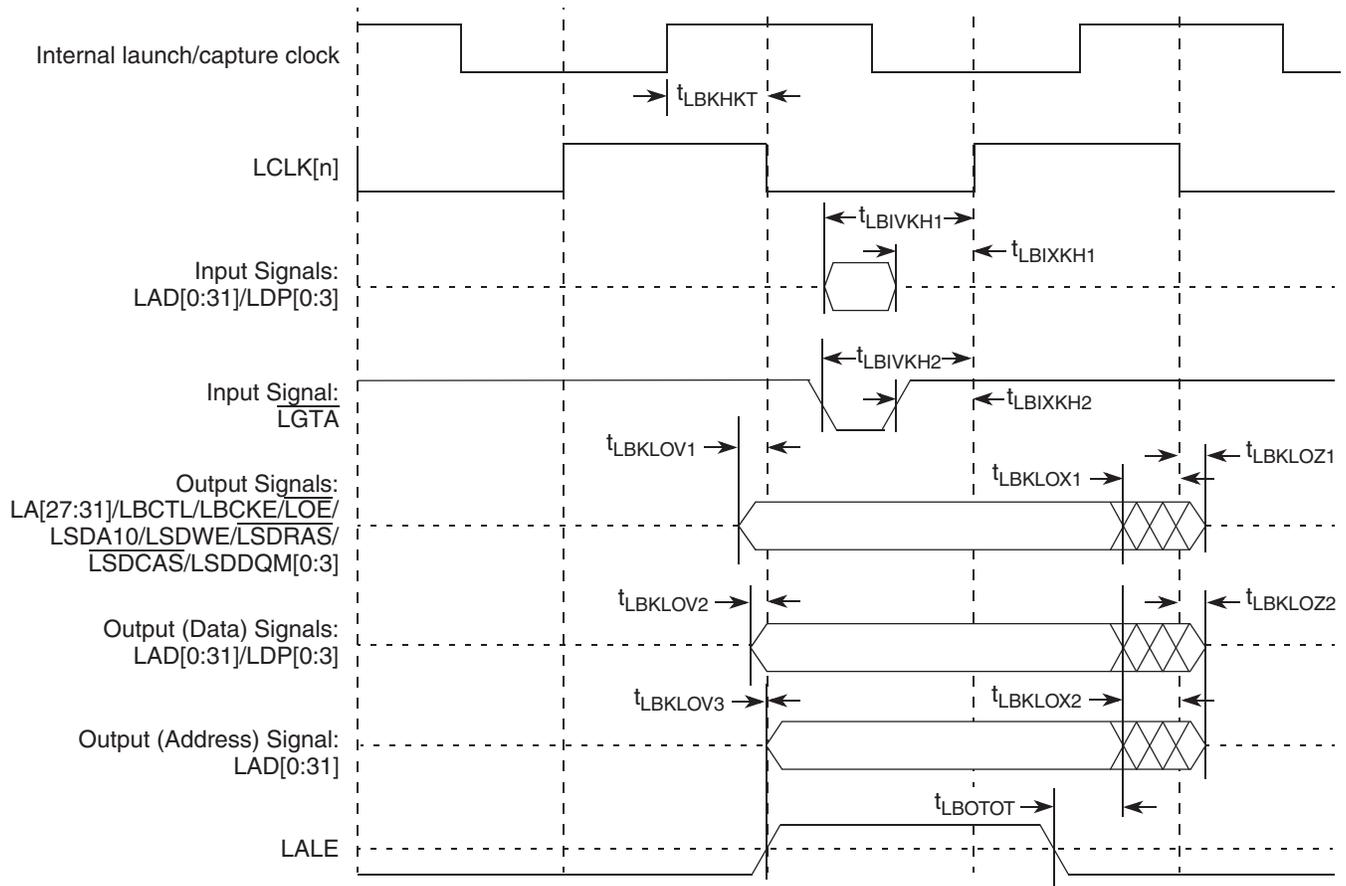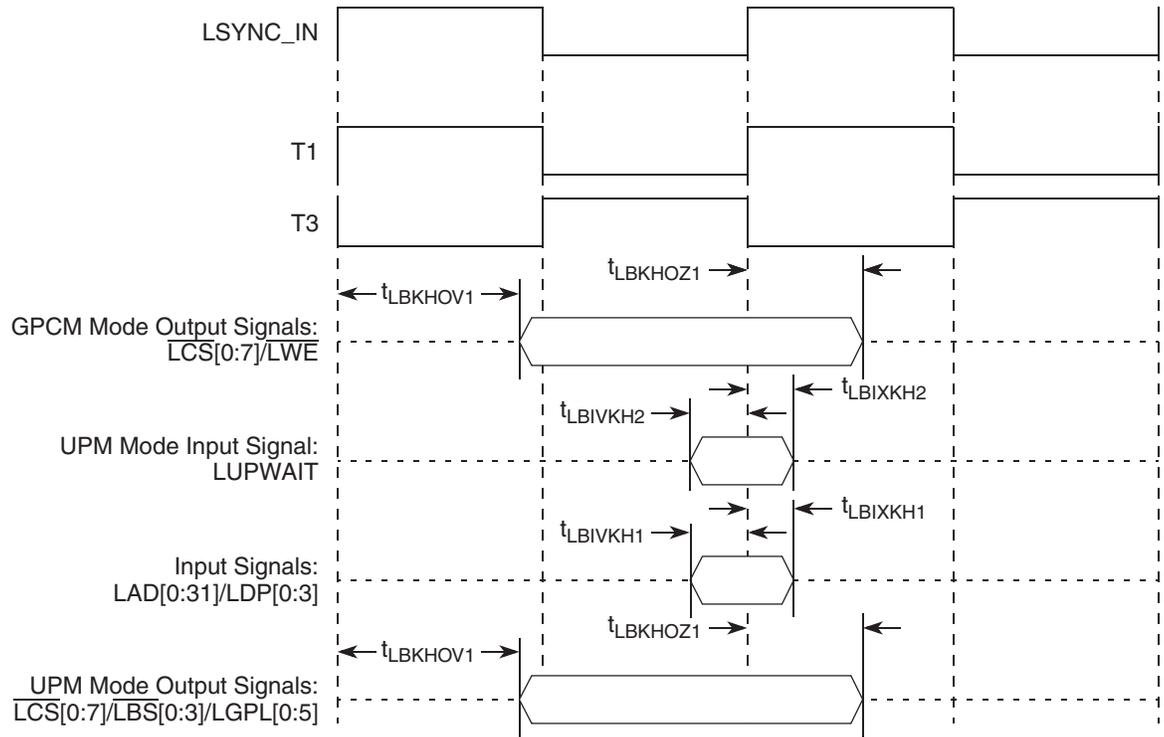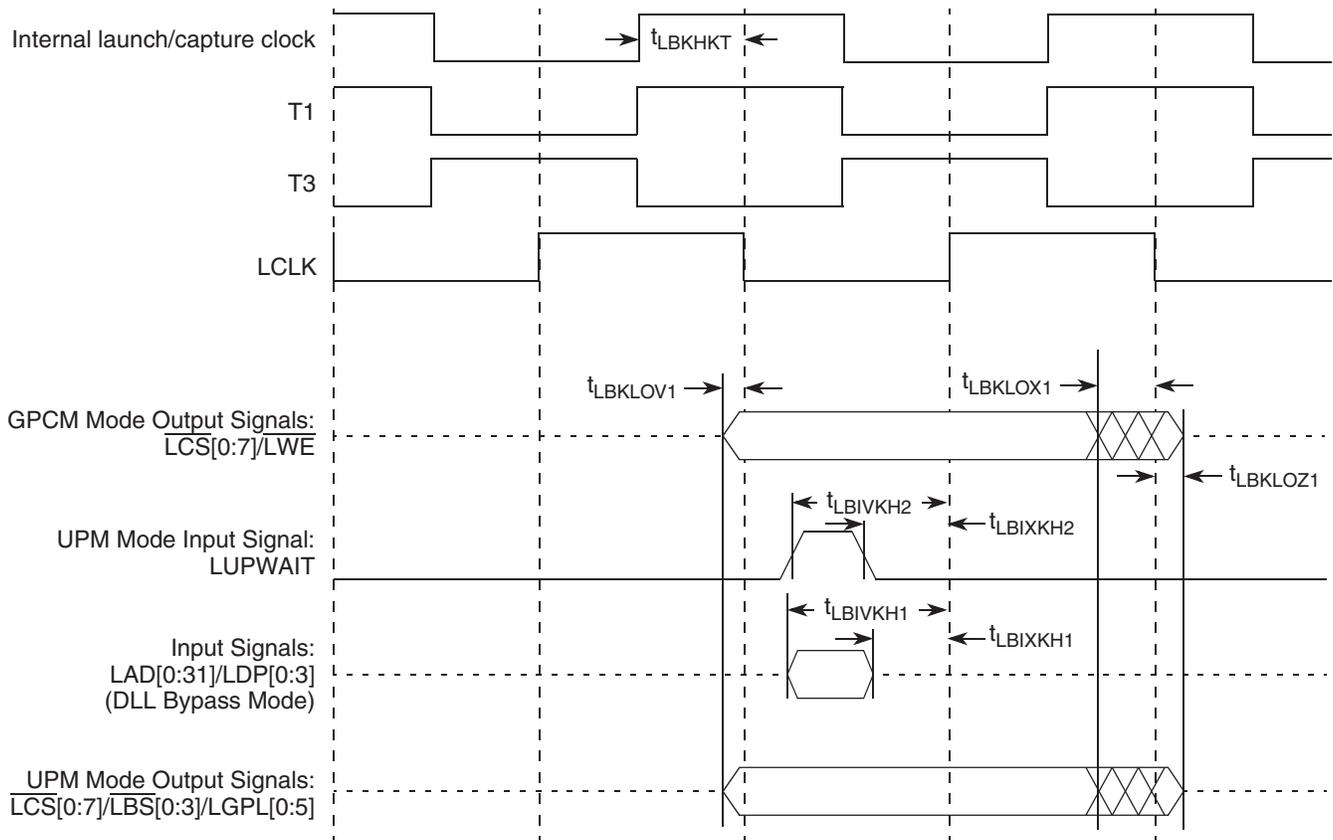
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Figure 9-5. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

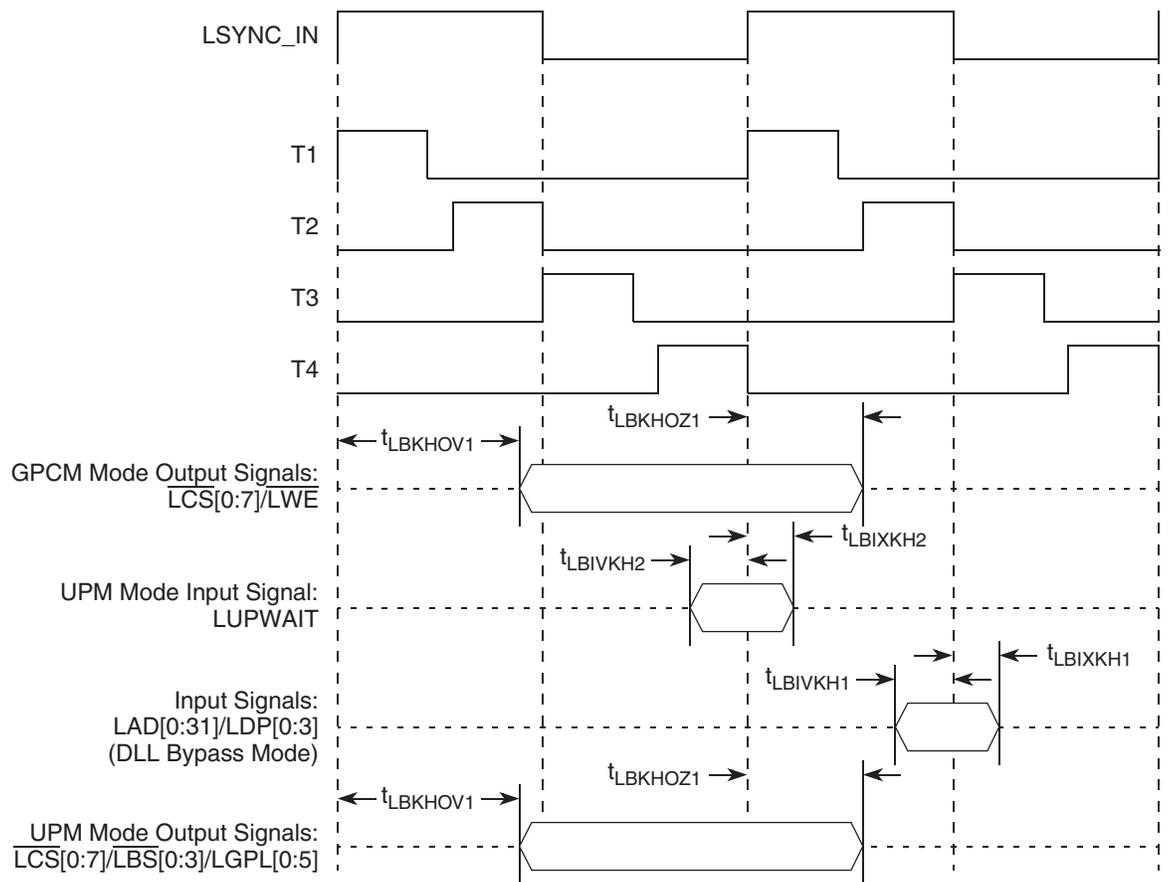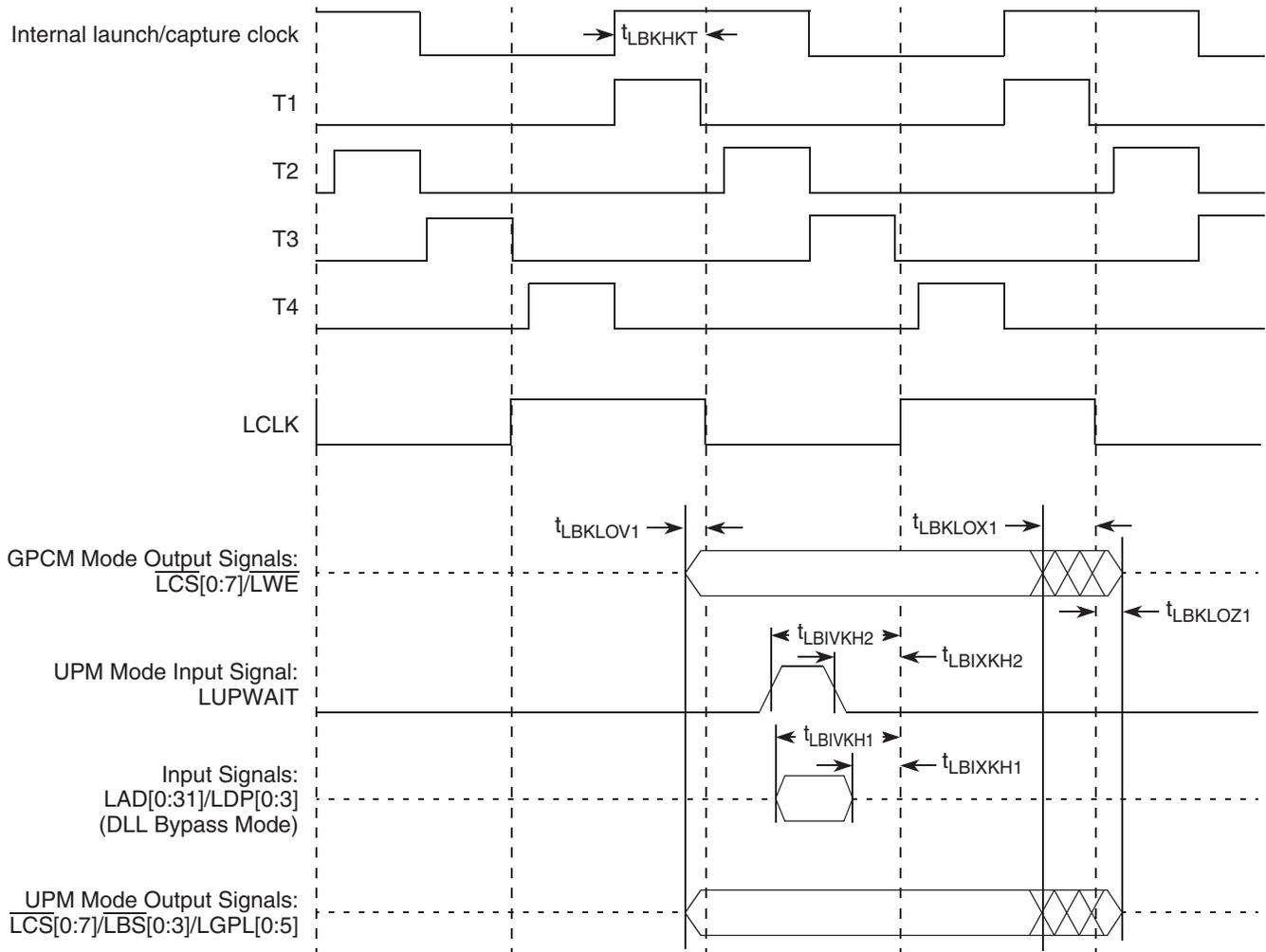**Figure 9-6.** Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Enabled)

Figure 9-7.   Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 or 8 (DLL Bypass Mode)

10. JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the PC8540. Table 10-1 provides the JTAG AC timing specifications as defined in Figure 12-1 on page 48 through Figure 13-1 on page 52.

Table 10-1. JTAG AC Timing Specifications (Independent of SYSCLK)[1] (At Recommended Operating Conditions (see Table 2-2 on page 8))

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	–	ns	
JTAG external clock pulse width measured at 1.4V	t_{JTKHKL}	15	–	ns	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	[6]
$\overline{TRST}$ assert time	t_{TRST}	25	–	ns	[3]
Input setup times: - Boundary-scan data - TMS, TDI	t_{JTDVKH} t_{JTIVKH}	4 0	– –	ns	[4]
Input hold times: - Boundary-scan data - TMS, TDI	t_{JTDXKH} t_{JTIXKH}	20 25	– –	ns	[4]
Valid times: - Boundary-scan data - TDO	t_{JTKLDV} t_{JTKLOV}	4 4	20 25	ns	[5]
Output hold times: - Boundary-scan data - TDO	t_{JTKLDX} t_{JTKLOX}			ns	[5]
JTAG external clock to output high impedance: - Boundary-scan data - TDO	t_{JTKLDZ} t_{JTKLOZ}	3 3	19 9	ns	[5][6]

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (see Figure 10-1 on page 43). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{(first two letters of functional block)(signal)(state) (reference)(state)}$ for inputs and $t_{(first two letters of functional block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design.

Figure 10-1 provides the AC test load for TDO and the boundary-scan outputs of the PC8540

Figure 10-1. AC Test Load for the JTAG Interface
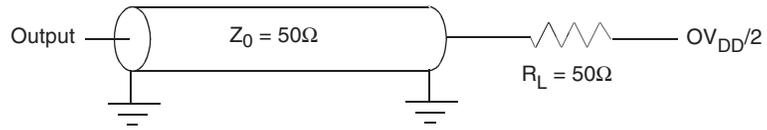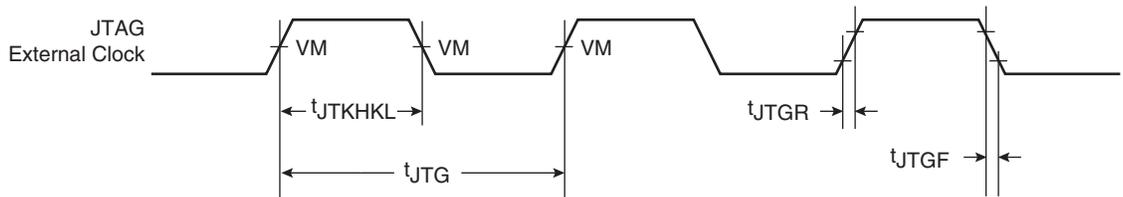

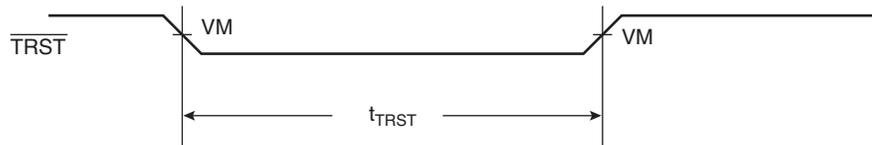Figure 10-2 provides the JTAG clock input timing diagram.

Figure 10-2. JTAG Clock Input Timing Diagram

Note: VM = Midpoint Voltage ($OV_{DD}/2$).
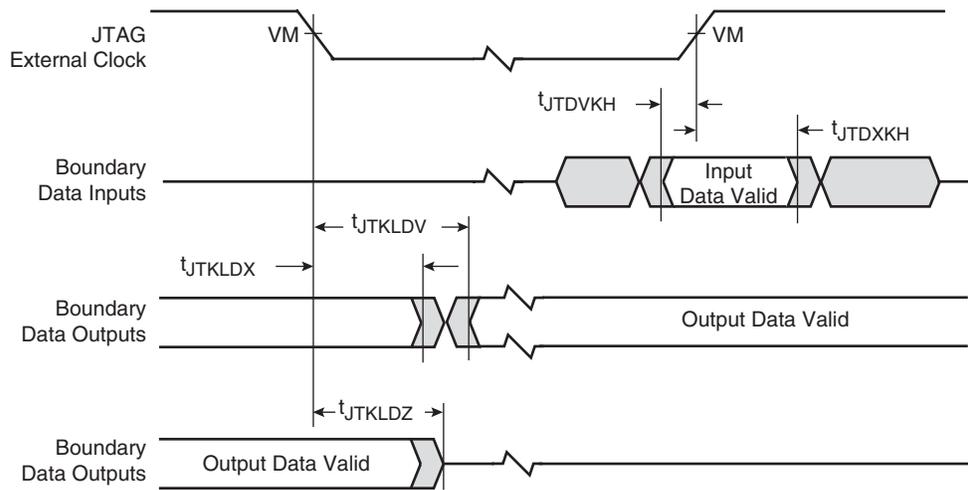
Figure 10-3 provides the $\overline{TRST}$ timing diagram.

Figure 10-3. $\overline{TRST}$ Timing Diagram

Note: VM = Midpoint Voltage ($OV_{DD}/2$).

Figure 10-4 provides the boundary-scan timing diagram.

Figure 10-4. Boundary-scan Timing Diagram

Note: VM = Midpoint Voltage ($OV_{DD}/2$).

Figure 10-5 provides the test access port timing diagram.

Figure 10-5. Test Access Port Timing Diagram
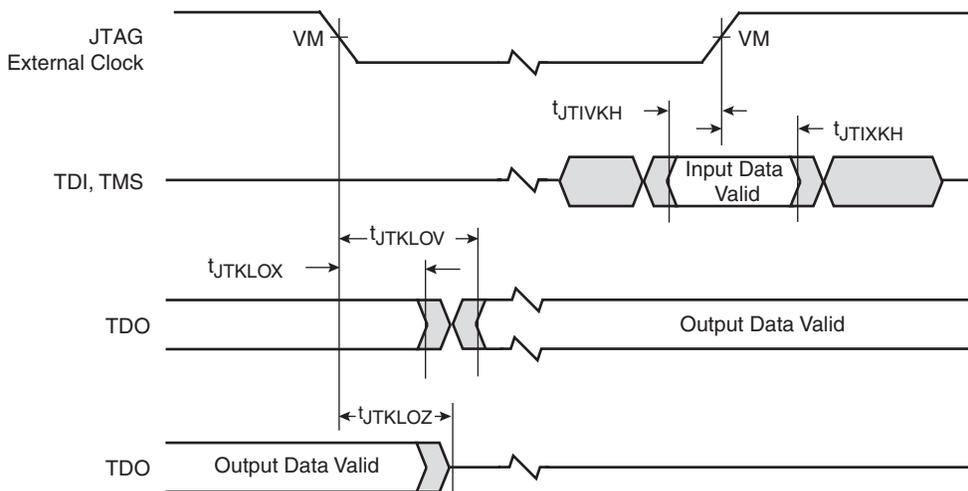
Note: VM = Midpoint Voltage ($OV_{DD}/2$)

11. I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the PC8540.

11.1 I²C DC Electrical Characteristics

Table 11-1 provides the DC electrical characteristics for the I²C interface of the PC8540.

Table 11-1. I²C DC Electrical Characteristics (At Recommended Operating Conditions with OV_{DD} of 3.3V ± 5%)

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	-0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	[1]
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	[2]
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$ (max)	I_I	-10	10	µA	[3]
Capacitance for each I/O pin	C_I		10	pF	

Notes: 1. Output voltage (open drain or open collector) condition = 3 mA sink current.

2. Refer to the PC8540 Integrated Processor Preliminary Reference Manual for information on the digital filter used.

3. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

11.2 I²C AC Electrical Specifications

Table 11-2 provides the AC timing parameters for the I²C interface of the PC8540.

Table 11-2. I²C AC Electrical Specifications (All values refer to V_{IH} (min) and V_{IL} (max) levels

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}[5]	1.3	–	µs
High period of the SCL clock	t_{I2CH}[5]	0.6	–	µs
Setup time for a repeated START condition	t_{I2SVKH}[5]	0.6	–	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}[5]	0.6	–	µs
Data setup time	t_{I2DVKH}[5]	100	–	ns
Data hold time: - CBUS[4] compatible masters - I²C bus devices	t_{I2DXKL}	– 0[2]	– 0.9[3]	µs
Set-up time for STOP condition	t_{I2PVKH}	0.6	–	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3		µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$		V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$		V

Notes: 1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I^{2}C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I^{2}C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I^{2}C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. PC8540 provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

4. C_B = capacitance of one bus line in pF.

5. Guaranteed by design.

Figure 11-1 provides the AC test load for the I^{2}C.
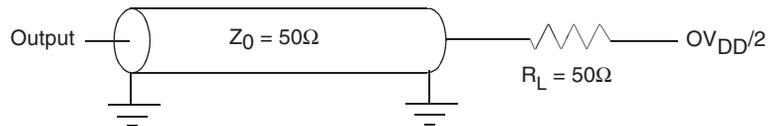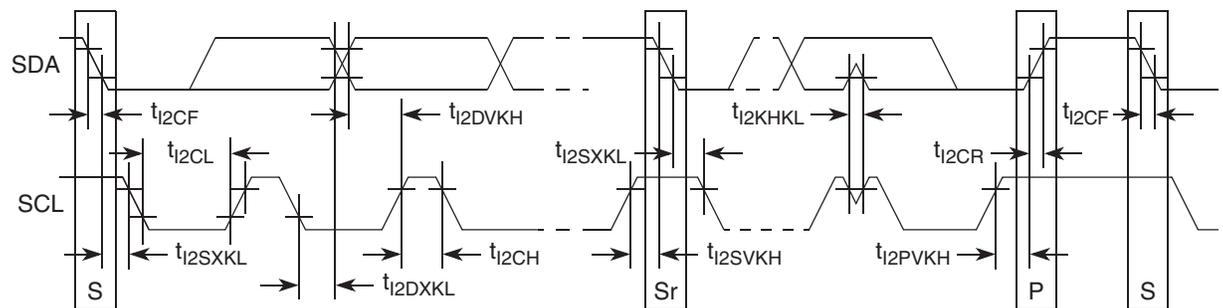
Figure 11-1. I^{2}C AC Test Load

Figure 11-2 shows the AC timing diagram for the I^{2}C bus.

Figure 11-2. I^{2}C Bus AC Timing Diagram

12. PCI/PCI-X

Table 12-1 on page 47 describes the DC and AC electrical specifications for the PCI/PCI-X bus of the PC8540.

12.1 PCI/PCI-X DC Electrical Characteristics

Table 12-1 provides the DC electrical characteristics for the PCI/PCI-X interface of the PC8540.

Table 12-1. PCI/PCI-X DC Electrical Characteristics[1]

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current (V_{IN}[2] = 0V or $V_{IN} = V_{DD}$)	I_{IN}	–	± 5	µA
High-level output voltage (OV_{DD} = min, I_{OH} = -100 µA)	V_{OH}	$OV_{DD} - 0.2$	–	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 µA)	V_{OL}	–	0.2	V

Notes: 1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.

2. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2-1 on page 7 and Table 2-2 on page 8.

12.2 PCI/PCI-X AC Electrical Specifications

This section describes the general AC timing parameters of the PCI/PCI-X bus of the PC8540. Note that the SYSCLK signal is used as the PCI input clock. Table 12-2 provides the PCI AC timing specifications at 66 MHz.

Table 12-2. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
SYSCLK to output valid	t_{PCKHOV}	–	6	ns	[2]
Output hold from SYSCLK	t_{PCKHOX}	2	–	ns	[2][9]
SYSCLK to output high impedance	t_{PCKHOZ}	–	14	ns	[2][3][10]
Input setup to SYSCLK	t_{PCIVKH}	3	–	ns	[2][4][9]
Input hold from SYSCLK	t_{PCIXKH}	0	–	ns	[2][4][9]
$\overline{REQ64}$ to $\overline{HRESET}$[9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	–	clocks	[5][6][10]
$\overline{HRESET}$ to $\overline{REQ64}$ hold time	t_{PCRHRX}	0	50	ns	[6][10]
$\overline{HRESET}$ high to first $\overline{FRAME}$ assertion	t_{PCRHF}	10		clocks	[7][10]

Notes: 1. Note that the symbols used for timing specifications herein follow the pattern of $t_{(first two letters of functional block)(signal)(state) (reference)(state)}$ for inputs and $t_{(first two letters of functional block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{PCIVKH} symbolizes PCI/PCI-X timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI/PCI-X timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.

2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.

3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

4. Input timings are measured at the pin.

5. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 15. "Clocking" on page 71.

6. The setup and hold time is with respect to the rising edge of $\overline{HRESET}$.

7. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.

8. The reset assertion timing requirement for $\overline{HRESET}$ is 100 µs.

9. Guaranteed by characterization.

10. Guaranteed by design.

Figure 12-1 provides the AC test load for PCI and PCI-X.

Figure 12-1. PCI/PCI-X AC Test Load
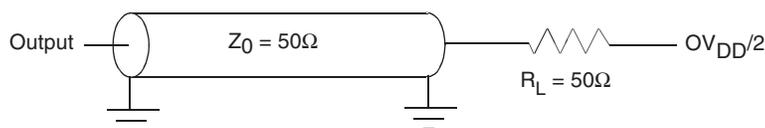
Figure 12-2 shows the PCI/PCI-X input AC timing conditions.

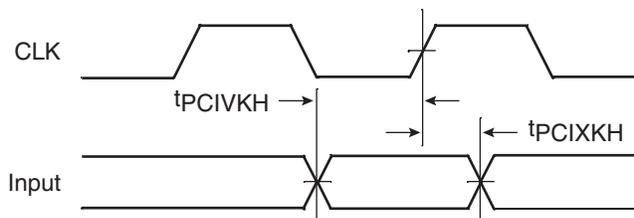**Figure 12-2.** PCI-PCI-X Input AC Timing Measurement Conditions

Figure 12-3 shows the PCI/PCI-X output AC timing conditions.

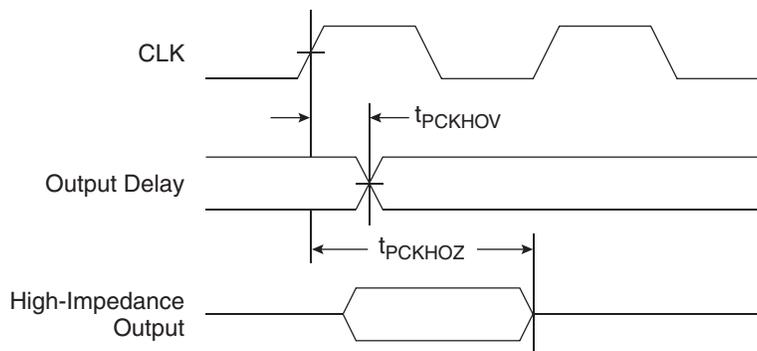**Figure 12-3.** PCI-PCI-X Output AC Timing Measurement Condition

Table 12-3 provides the PCI-X AC timing specifications at 66 MHz.

Table 12-3. PCI-X AC Timing Specifications at 66 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	–	3.8	ns	(1)(2)(3)(7)(8)
Output hold from SYSCLK	t_{PCKHOX}	0.7	–	ns	(1)(10)
SYSCLK to output high impedance	t_{PCKHOZ}	–	7	ns	(1)(4)(8)(11)
Input setup time to SYSCLK	t_{PCIVKH}	1.7	–	ns	(3)(5)
Input hold time from SYSCLK	t_{PCIXKH}	0.5	–	ns	(10)
$\overline{REQ64}$ to $\overline{HRESET}$ setup time	t_{PCRVRH}	10	–	clocks	(11)
$\overline{HRESET}$ to $\overline{REQ64}$ hold time	t_{PCRHRX}	0	50	ns	(11)
$\overline{HRESET}$ high to first $\overline{FRAME}$ assertion	t_{PCRHFV}	10	–	clocks	(9)(11)
PCI-X initialization pattern to $\overline{HRESET}$ setup time	t_{PCIVRH}	10	–	clocks	(11)
$\overline{HRESET}$ to PCI-X initialization pattern hold time	t_{PCRHIX}	0	50	ns	(6)(11)

Notes: 1. See the timing measurement conditions in the *PCI-X 1.0a Specification*.

2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.

3. Setup time for point-to-point signals applies to $\overline{REQ}$ and $\overline{GNT}$ only. All other signals are bused.

4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.

6. Maximum value is also limited by delay to the first transaction (time for $\overline{HRESET}$ high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of $\overline{HRESET}$ must be negated no later than two clocks before the first $\overline{FRAME}$ and must be floated no later than one clock before $\overline{FRAME}$ is asserted.

7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.

8. Device must meet this specification independent of how many outputs switch simultaneously.

9. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification*.

10. Guaranteed by characterization.

11. Guaranteed by design.

Table 12-4. PCI-X AC Timing Specifications at 133 MHz

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	t_{PCKHOV}	–	3.8	ns	(1)(2)(3)(7)(8)
Output hold from SYSCLK	t_{PCKHOX}	0.7	–	ns	(1)(11)
SYSCLK to output high impedance	t_{PCKHOZ}	–	7	ns	(1)(4)(8)(12)
Input setup time to SYSCLK	t_{PCIVKH}	1.4	–	ns	(3)(5)(9)(11)
Input hold time from SYSCLK	t_{PCIXKH}	0.5	–	ns	(11)
$\overline{REQ64}$ to $\overline{HRESET}$ setup time	t_{PCRVRH}	10	–	clocks	(12)
$\overline{HRESET}$ to $\overline{REQ64}$ hold time	t_{PCRHRX}	0	50	ns	(12)
$\overline{HRESET}$ high to first $\overline{FRAME}$ assertion	t_{PCRHFV}	10	–	clocks	(10)(12)
PCI-X initialization pattern to $\overline{HRESET}$ setup time	t_{PCIVRH}	10	–	clocks	(12)
$\overline{HRESET}$ to PCI-X initialization pattern hold time	t_{PCRHIX}	0	50	ns	(6)(12)

Notes: 1. See the timing measurement conditions in the *PCI-X 1.0a Specification*.

2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.

3. Setup time for point-to-point signals applies to $\overline{REQ}$ and $\overline{GNT}$ only. All other signals are bused.

4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.

6. Maximum value is also limited by delay to the first transaction (time for $\overline{HRESET}$ high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of $\overline{HRESET}$ must be negated no later than two clocks before the first $\overline{FRAME}$ and must be floated no later than one clock before $\overline{FRAME}$ is asserted.

7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.

8. Device must meet this specification independent of how many outputs switch simultaneously.

9. The timing parameter t_{PCIVKH} is a minimum of 1.4 ns rather than the minimum of 1.2 ns in the *PCI-X 1.0a Specification.*

10. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI-X 1.0a Specification.*

11. Guaranteed by characterization.

12. Guaranteed by design.

13. RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the PC8540.

13.1 RapidIO DC Electrical Characteristics

RapidIO driver and receiver DC electrical characteristics are provided in Table 13-1 and Table 13-2, respectively.

Table 13-1. RapidIO 8/16 LP-LVDS Driver DC Electrical Characteristics (At Recommended Operating Conditions with OV_{DD} of 3.3V ± 5%)

Characteristic	Symbol	Min	Max	Unit	Notes
Differential output high voltage	V_{OHD}	247	454	mV	[1][2]
Differential output low voltage	V_{OLD}	-454	-247	mV	[1][2]
Differential offset voltage	ΔV_{OSD}		50	mV	[1][3]
Output high common mode voltage	V_{OHCM}	1.125	1.375	V	[1][4]
Output low common mode voltage	V_{OLCM}	1.125	1.375	V	[1][5]
Common mode offset voltage	Δ_{VOSCM}		50	mV	[1][6]
Differential termination	R_{TERM}	90	220	W	
Short circuit current (either output)	$|I_{SS}|$		24	mA	[7]
Bridged short circuit current	$|I_{SB}|$		12	mA	[8]

Notes:
1. Bridged 100Ω load.
2. See Figure 13-7 on page 60 (a).
3. Differential offset voltage = $|V_{OHD} + V_{OLD}|$. See Figure 13-7 on page 60.
4. $V_{OHCM} = (V_{OA} + V_{OB})/2$ when measuring V_{OHD}.
5. $V_{OLCM} = (V_{OA} + V_{OB})/2$ when measuring V_{OLD}.
6. Common mode offset $\Delta V_{OSCM} = |V_{OHCM} - V_{OLCM}|$. See Figure 13-7 on page 60.
7. Outputs shorted to V_{DD} or GND.
8. Outputs shorted together.

Table 13-2. RapidIO 8/16 LP-LVDS Receiver DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit	Notes
Voltage at either input	V_I	0	2.4	V	
Differential input high voltage	V_{IHD}	100	600	mV	[1]
Differential input low voltage	V_{ILD}	-600	-100	mV	[1]
Common mode input range (referenced to receiver ground)	V_{ICM}	0.050	2.350	V	[2]
Input differential resistance	R_{IN}	90	110	W	

Notes:
1. Over the common mode range.
2. Limited by V_I. See Figure 16-2 on page 75.

Figure 13-1. DC Driver Signal Levels

$V_{OD} = V_{OA} - V_{OB}$

(a)

Differential Specifications **(b)**

Common-Mode Specifications **(c)**
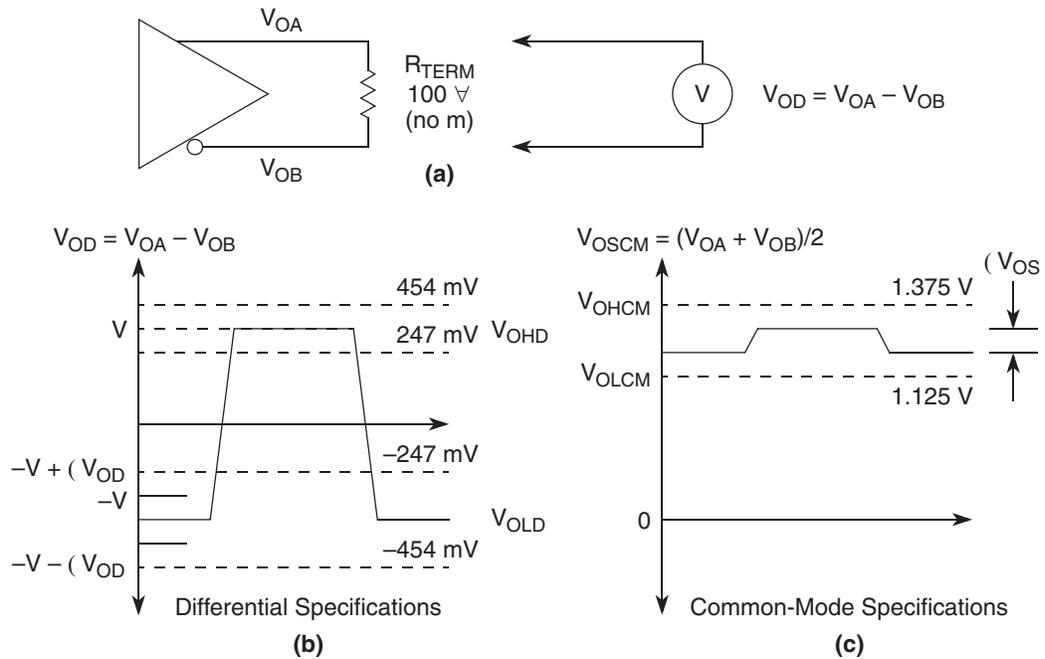
Note: VOA refers to voltage at output A; VOB refers to voltage at output B.

13.2 RapidIO AC Electrical Specifications

This section contains the AC electrical specifications for a RapidIO 8/16 LP-LVDS device. The interface defined is a parallel differential low-power high-speed signal interface. Note that the source of the transmit clock on the RapidIO interface is dependent on the settings of the LGPL[0:1] signals at reset. Note that the default setting makes the core complex bus (CCB) clock the source of the transmit clock.

13.3 RapidIO Concepts and Definitions

This section specifies signals using differential voltages. Figure 13-8 on page 61 shows how the signals are defined. The figure shows waveforms for either a transmitter output (TD and $\overline{TD}$) or a receiver input (RD and $\overline{RD}$). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- The transmitter output and receiver input signals TD, $\overline{TD}$, RD, and $\overline{RD}$ each have a peak-to-peak swing of A-B volts.
- The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} - V\overline{TD}$.
- The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} - V\overline{RD}$.
- The differential output signal of the transmitter or input signal of the receiver, ranges from A - B volts to -(A - B) volts.
- The peak differential signal of the transmitter output or receiver input, is A - B volts.
- The peak-to-peak differential signal of the transmitter output or receiver input, is 2 × (A - B) volts.

Figure 13-2. Differential Peak-to-Peak Voltage of Transmitter or Receiver
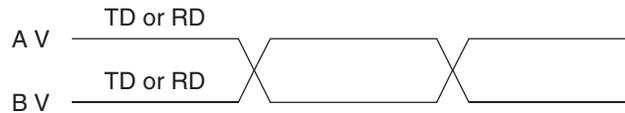
To illustrate these definitions using numerical values, consider the case where a LVDS transmitter has a common mode voltage of 1.2V and each signal has a swing that goes between 1.4 and 1V. Using these values, the peak-to-peak voltage swing of the signals TD, $\overline{TD}$, RD, and $\overline{RD}$ is 400 mV. The differential signal ranges between 400 and -400 mV. The peak differential signal is 400 mV, and the peak-to-peak differential signal is 800 mV.

A timing edge is the zero-crossing of a differential signal. Each skew timing parameter on a parallel bus is synchronously measured on two signals relative to each other in the same cycle, such as data to data, data to clock, or clock to clock. A skew timing parameter may be relative to the edge of a signal or to the middle of two sequential edges.

Static skew represents the timing difference between signals that does not vary over time regardless of system activity or data pattern. Path length differences are a primary source of static skew.

Dynamic skew represents the amount of timing difference between signals that is dependent on the activity of other signals and varies over time. Crosstalk between signals is a source of dynamic skew.

Eye diagrams and compliance masks are a useful way to visualize and specify driver and receiver performance. This technique is used in several serial bus specifications. An example compliance mask is shown in Figure 13-9 on page 61. The key difference in the application of this technique for a parallel bus is that the data is source synchronous to its bus clock while serial data is referenced to its embedded clock. Eye diagrams reveal the quality (cleanness, openness, goodness) of a driver output or receiver input. An advantage of using an eye diagram and a compliance mask is that it allows specifying the quality of a signal without requiring separate specifications for effects such as rise time, duty cycle distortion, data dependent dynamic skew, random dynamic skew, etc. This allows the individual semiconductor manufacturer maximum flexibility to trade off various performance criteria while keeping the system performance constant.

In using the eye pattern and compliance mask approach, the quality of the signal is specified by the compliance mask. The mask specifies the maximum permissible magnitude of the signal and the minimum permissible eye opening. The eye diagram for the signal under test is generated according to the specification. Compliance is determined by whether the compliance mask can be positioned over the eye diagram such that the eye pattern falls entirely within the unshaded portion of the mask.

Serial specifications have clock encoded with the data, but the LP-LVDS physical layer defined by RapidIO is a source synchronous parallel port so additional specifications to include effects that are not found in serial links are required. Specifications for the effect of bit to bit timing differences caused by static skew have been added and the eye diagrams specified are measured relative to the associated clock in order to include clock to data effects. With the transmit output (or receiver input) eye diagram, the user can determine if the transmitter output (or receiver input) is compliant with an oscilloscope with the appropriate software.

Figure 13-3. Example Compliance Mask
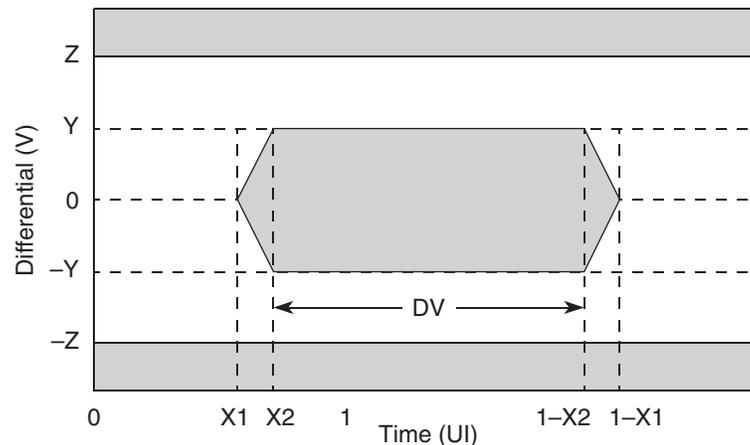
Y = minimum data valid amplitude

Z = maximum amplitude

1 UI = 1 unit interval = 1/baud rate

X1 = end of zero crossing region

X2 = beginning of data valid window

DV = data valid window = $1 - 2 \times X2$

The waveform of the signal under test must fall within the unshaded area of the mask to be compliant. Different masks are used for the driver output and the receiver input allowing each to be separately specified.

13.3.1 RapidIO Driver AC Timing Specifications

Driver AC timing specifications are provided in Table 13-3, Table 13-4, and Table 13-5. A driver shall comply with the specifications for each data rate/frequency for which operation of the driver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The output of a driver shall be connected to a 100Ω, ± 1%, differential (bridged) resistive load.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7]).

Table 13-3. RapidIO Driver AC Timing Specifications: 500 Mbps Data Rate

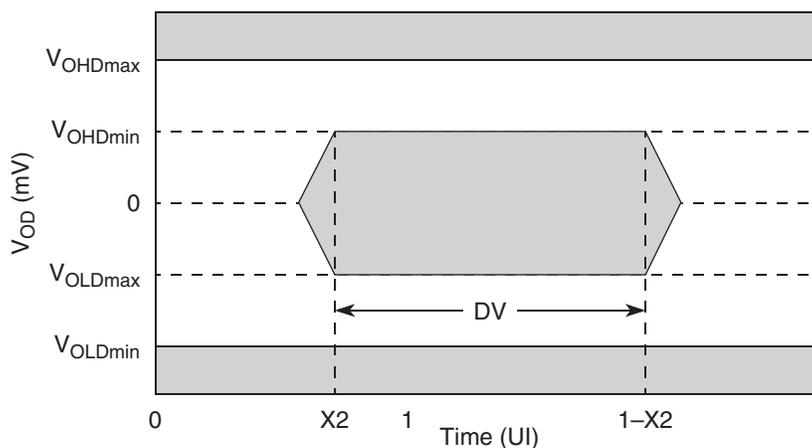| Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential output high voltage	V_{OHD}	200	540	mV	(1)
Differential output low voltage	V_{OLD}	-540	-200	mV	(1)
Duty cycle	DC	48	52	%	(2)(6)
V_{OD} rise time, 20%–80% of peak-to-peak differential signal swing	t_{FALL}	200	–	ps	(3)(6)
V_{OD} fall time, 20%–80% of peak-to-peak differential signal swing	t_{RISE}	200	–	ps	(6)
Data valid	DV	1260	–	ps	
Skew of any two data outputs	t_{DPAIR}	–	180	ps	(4)(6)
Skew of single data outputs to associated clock	$t_{SKEW,PAIR}$	-180	180	ps	(5)(6)

Notes: 1. 1.See Figure 14-1 on page 63.
2. Requires ± 100 ppm long term frequency stability.
3. Measured at V_{OD} = 0V.
4. Measured using the RapidIO transmit mask shown in Figure 14-1 on page 63.
5. See Figure 16-3 on page 75.
6. Guaranteed by design.

Table 13-4. RapidIO Driver AC Timing Specifications: 750 Mbps Data Rate

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential output high voltage	V_{OHD}	200	540	mV	(1)
Differential output low voltage	V_{OLD}	-540	-200	mV	(1)
Duty cycle	DC	48	52	%	(2)(6)
V_{OD} rise time, 20%–80% of peak-to-peak differential signal swing	t_{FALL}	133	–	ps	(3)(6)
V_{OD} fall time, 20%–80% of peak-to-peak differential signal swing	t_{RISE}	133	–	ps	(6)
Data valid	DV	800	–	ps	
Skew of any two data outputs	t_{DPAIR}	–	133	ps	(4)(6)
Skew of single data outputs to associated clock	$t_{SKEW,PAIR}$	-133	133	ps	(5)(6)

Notes: 1. See Figure 14-1 on page 63.
2. Requires ± 100 ppm long term frequency stability.
3. Measured at V_{OD} = 0V.
4. Measured using the RapidIO transmit mask shown in Figure 14-1 on page 63.
5. See Figure 16-3 on page 75.
6. Guaranteed by design.

Table 13-5. RapidIO Driver AC Timing Specifications: 1 Gbps Data Rate

Characteristic	Symbol	Range Min	Range Max	Unit	Notes
Differential output high voltage	V_{OHD}	200	540	mV	(1)
Differential output low voltage	V_{OLD}	-540	-200	mV	(1)
Duty cycle	DC	48	52	%	(2)(6)
V_{OD} rise time, 20%–80% of peak-to-peak differential signal swing	t_{FALL}	100	–	ps	(3)(6)
V_{OD} fall time, 20%–80% of peak-to-peak differential signal swing	t_{RISE}	100	–	ps	(6)
Data valid	DV	575	–	ps	
Skew of any two data outputs	t_{DPAIR}	–	100	ps	(4)(6)
Skew of single data outputs to associated clock	$t_{SKEW,PAIR}$	-100	100	ps	(5)(6)

Notes: 1. See Figure 14-1 on page 63.

2. Requires ± 100 ppm long term frequency stability.

3. Measured at V_{OD} = 0V.

4. Measured using the RapidIO transmit mask shown in Figure 14-1 on page 63.

5. See Figure 16-3 on page 75.

6. Guaranteed by design.

The compliance of driver output signals TD[0:15] and TFRAME with their minimum data valid window (DV) specification shall be determined by generating an eye pattern for each of the data signals and comparing the eye pattern of each data signal with the RapidIO transmit mask shown in Figure 14-1 on page 63. The value of X2 used to construct the mask shall be $(1 – DV_{min})/2$. A signal is compliant with the data valid window specification if the transmit mask can be positioned on the signal's eye pattern such that the eye pattern falls entirely within the unshaded portion of the mask.

Figure 13-4. RapidIO Transmit Mask

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The eye pattern for a data signal is generated by making a large number of recordings of the signal and then overlaying the recordings. The number of recordings used to generate the eye shall be large enough that further increasing the number of recordings used does not cause the resulting eye pattern to change from one that complies with the RapidIO transmit mask to one that does not. Each data signal in the interface shall be carrying random or pseudo-random data when the recordings are made. If pseudo-random data is used, the length of the pseudo-random sequence (repeat length) shall be long enough that increasing the length of the sequence does not cause the resulting eye pattern to change from one that complies with the RapidIO transmit mask to one that does not comply with the mask. The data carried by any given data signal in the interface may not be correlated with the data carried by any other data signal in the interface. The zero-crossings of the clock associated with a data signal shall be used as the timing reference for aligning the multiple recordings of the data signal when the recordings are overlaid.

While the method used to make the recordings and overlay them to form the eye pattern is not specified, the method used shall be demonstrably equivalent to the following method. The signal under test is repeatedly recorded with a digital oscilloscope in infinite persistence mode. Each recording is triggered by a zero-crossing of the clock associated with the data signal under test. Roughly half of the recordings are triggered by positive-going clock zero-crossings and roughly half are triggered by negative-going clock zero-crossings. Each recording is at least 1.9 UI in length (to ensure that at least one complete eye is formed) and begins 0.5 UI before the trigger point (0.5 UI before the associated clock zero-crossing). Depending on the length of the individual recordings used to generate the eye pattern, one or more complete eyes will be formed. Regardless of the number of eyes, the eye whose center is immediately to the right of the trigger point is the eye used for compliance testing.

An example of an eye pattern generated using the above method with recordings 3 UI in length is shown in Figure 13-5. In this example, there is no skew between the signal under test and the associated clock used to trigger the recordings. If skew was present, the eye pattern would be shifted to the left or right relative to the oscilloscope trigger point.

Figure 13-5. Example Driver Output Eye Pattern
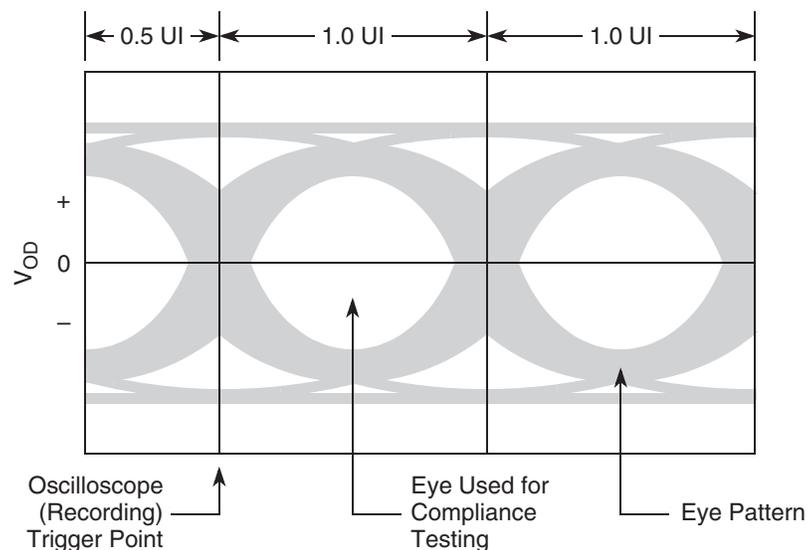
13.3.2 RapidIO Receiver AC Timing Specifications

The RapidIO receiver AC timing specifications are provided in Table 13-6. A receiver shall comply with the specifications for each data rate/frequency for which operation of the receiver is specified. Unless otherwise specified, these specifications are subject to the following conditions.

- The specifications apply over the supply voltage and ambient temperature ranges specified by the device vendor.
- The specifications apply for any combination of data patterns on the data signals.
- The specifications apply over the receiver common mode and differential input voltage ranges.
- Clock specifications apply only to clock signals.
- Data specifications apply only to data signals (FRAME, D[0:7]).

Table 13-6. RapidIO Receiver AC Timing Specifications: 500 Mbps Data Rate

Characteristic	Symbol	Range Min	Range Max	Unit	Notes
Duty cycle of the clock input	DC	47	53	%	( )(11)
Data valid	DV	1080		ps	(8)
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}		380	ps	(9)
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	-300	300	ps	(10)

7. Measured at V_{ID} = 0V.
8. Measured using the RapidIO receive mask shown in Figure 13-6 on page 59.
9. See Figure 16-3 on page 75.
10. See Figure 16-2 on page 75 and Figure 16-3 on page 75.
11. Guaranteed by design.

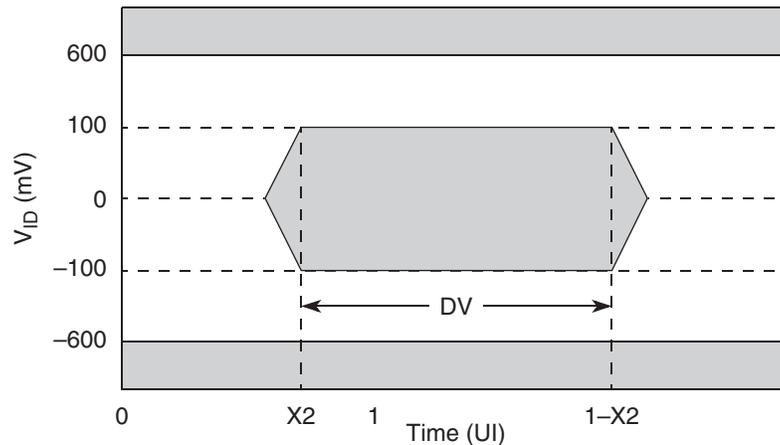**Table 13-7.** RapidIO Receiver AC Timing Specifications: 750 Mbps Data Rate

Characteristic	Symbol	Range Min	Range Max	Unit	Notes
Duty cycle of the clock input	DC	47	53	%	(1)(5)
Data valid	DV	600		ps	(2)
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}		400	ps	(3)
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	-267	267	ps	(4)

Notes: 1. Measured at V_{ID} = 0V.
2. Measured using the RapidIO receive mask shown in Figure 13-6 on page 59.
3. See Figure 16-3 on page 75.
4. See Figure 16-2 on page 75 and Figure 16-3 on page 75.
5. Guaranteed by design.

Table 13-8. RapidIO Receiver AC Timing Specifications: 1 Gbps Data Rate

Characteristic	Symbol	Range Min	Range Max	Unit	Notes
Duty cycle of the clock input	DC	47	53	%	(1)(5)
Data valid	DV	425		ps	(2)
Allowable static skew between any two data inputs within a 8-/9-bit group	t_{DPAIR}		300	ps	(3)
Allowable static skew of data inputs to associated clock	$t_{SKEW,PAIR}$	-200	200	ps	(4)

Notes: 1. Measured at $V_{ID} = 0V$.

2. Measured using the RapidIO receive mask shown in Figure 13-6 on page 59.

3. See Figure 16-3 on page 75.

4. See Figure 16-2 on page 75 and Figure 16-3 on page 75.

5. Guaranteed by design.

The compliance of receiver input signals RD[0:15] and RFRAME with their minimum data valid window (DV) specification shall be determined by generating an eye pattern for each of the data signals and comparing the eye pattern of each data signal with the RapidIO receive mask shown in Figure 13-6 on page 59. The value of X2 used to construct the mask shall be $(1 - DV_{min})/2$. The ± 100 mV minimum data valid and ± 600 mV maximum input voltage values are from the DC specification. A signal is compliant with the data valid window specification if and only if the receive mask can be positioned on the signal's eye pattern such that the eye pattern falls entirely within the unshaded portion of the mask.

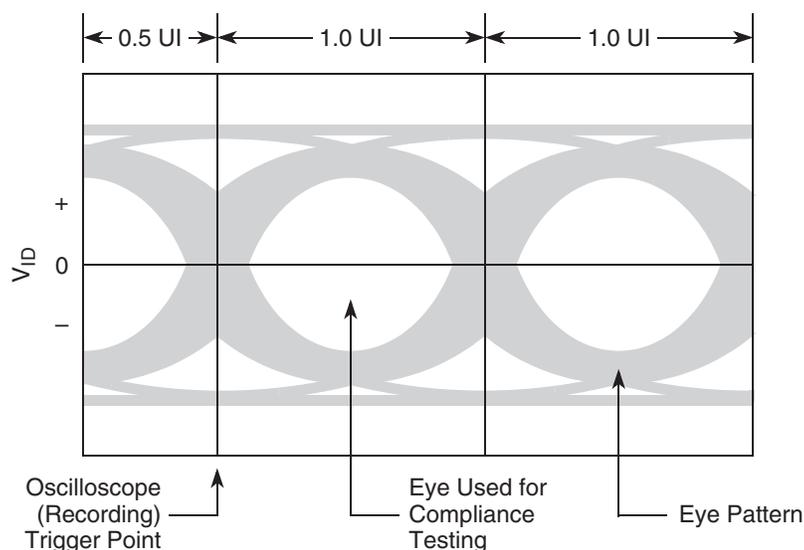**Figure 13-6.** RapidIO Receive Mask

The eye pattern for a data signal is generated by making a large number of recordings of the signal and then overlaying the recordings. The number of recordings used to generate the eye shall be large enough that further increasing the number of recordings used does not cause the resulting eye pattern to change from one that complies with the RapidIO receive mask to one that does not. Each data signal in the interface shall be carrying random or pseudo-random data when the recordings are made.

If pseudo-random data is used, the length of the pseudo-random sequence (repeat length) shall be long enough that increasing the length of the sequence does not cause the resulting eye pattern to change from one that complies with the RapidIO receive mask to one that does not comply with the mask. The data carried by any given data signal in the interface may not be correlated with the data carried by any other data signal in the interface. The zero-crossings of the clock associated with a data signal shall be used as the timing reference for aligning the multiple recordings of the data signal when the recordings are overlaid.

While the method used to make the recordings and overlay them to form the eye pattern is not specified, the method used shall be demonstrably equivalent to the following method. The signal under test is repeatedly recorded with a digital oscilloscope in infinite persistence mode. Each recording is triggered by a zero-crossing of the clock associated with the data signal under test. Roughly half of the recordings are triggered by positive-going clock zero-crossings and roughly half are triggered by negative-going clock zero-crossings. Each recording is at least 1.9 UI in length (to ensure that at least one complete eye is formed) and begins 0.5 UI before the trigger point (0.5 UI before the associated clock zero-crossing). Depending on the length of the individual recordings used to generate the eye pattern, one or more complete eyes will be formed. Regardless of the number of eyes, the eye whose center is immediately to the right of the trigger point is the eye used for compliance testing.

An example of an eye pattern generated using the above method with recordings 3 UI in length is shown in . In this example, there is no skew between the signal under test and the associated clock used to trigger the recordings. If skew was present, the eye pattern would be shifted to the left or right relative to the oscilloscope trigger point.

Figure 13-7. Example Receiver Input Eye Pattern

shows the definitions of the data to clock static skew parameter $t_{SKEW,PAIR}$ and the data valid window parameter DV. The data and frame bits are those that are associated with the clock. The figure applies for all zero-crossings of the clock. All of the signals are differential signals. V_D represents V_{OD} for the transmitter and V_{ID} for the receiver. The center of the eye is defined as the midpoint of the region in which the magnitude of the signal voltage is greater than or equal to the minimum DV voltage.
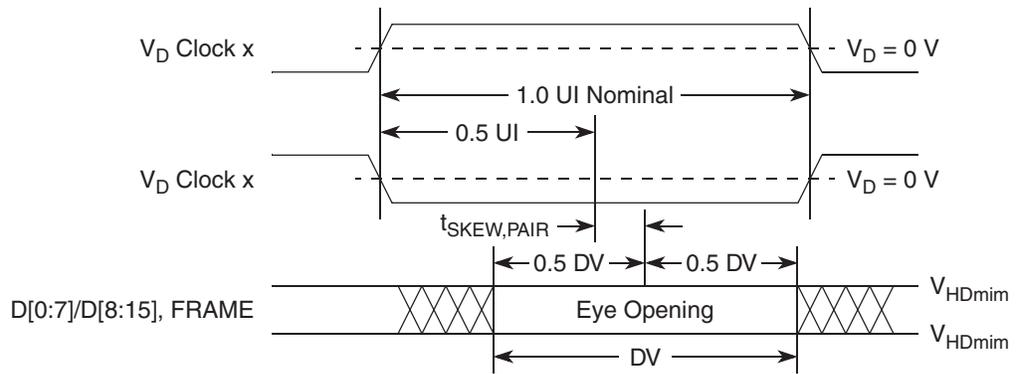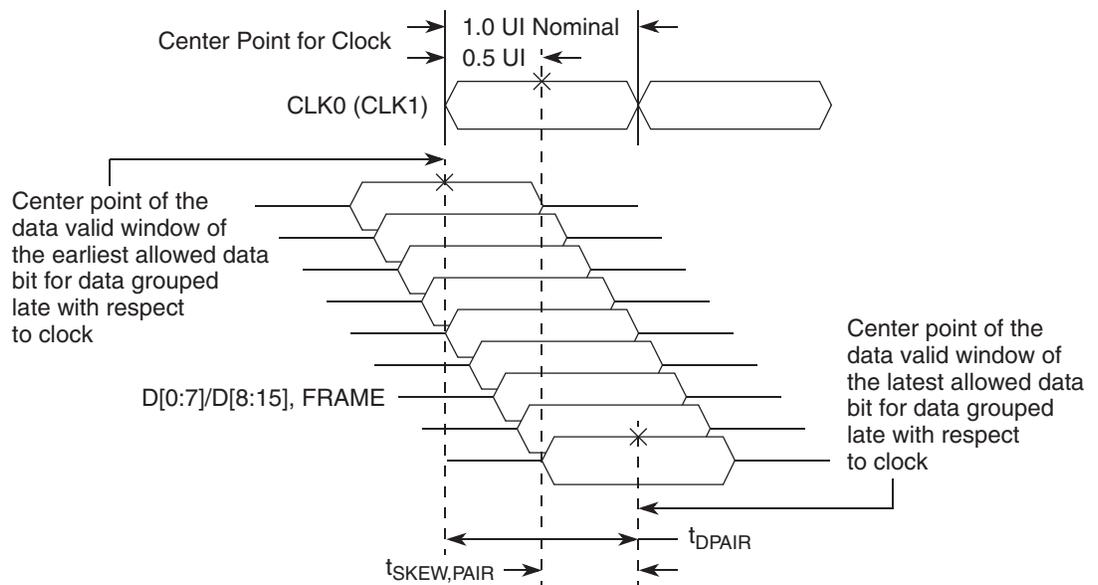
Figure 13-8. Data to Clock Skew

[Figure 16-3 on page 75](#) shows the definition of the data to data static skew parameter t_{DPAIR} and how the skew parameters are applied.

Figure 13-9. Static Skew Diagram

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14. Package and Pin Listings

This section details package parameters, pin assignments, and dimensions.
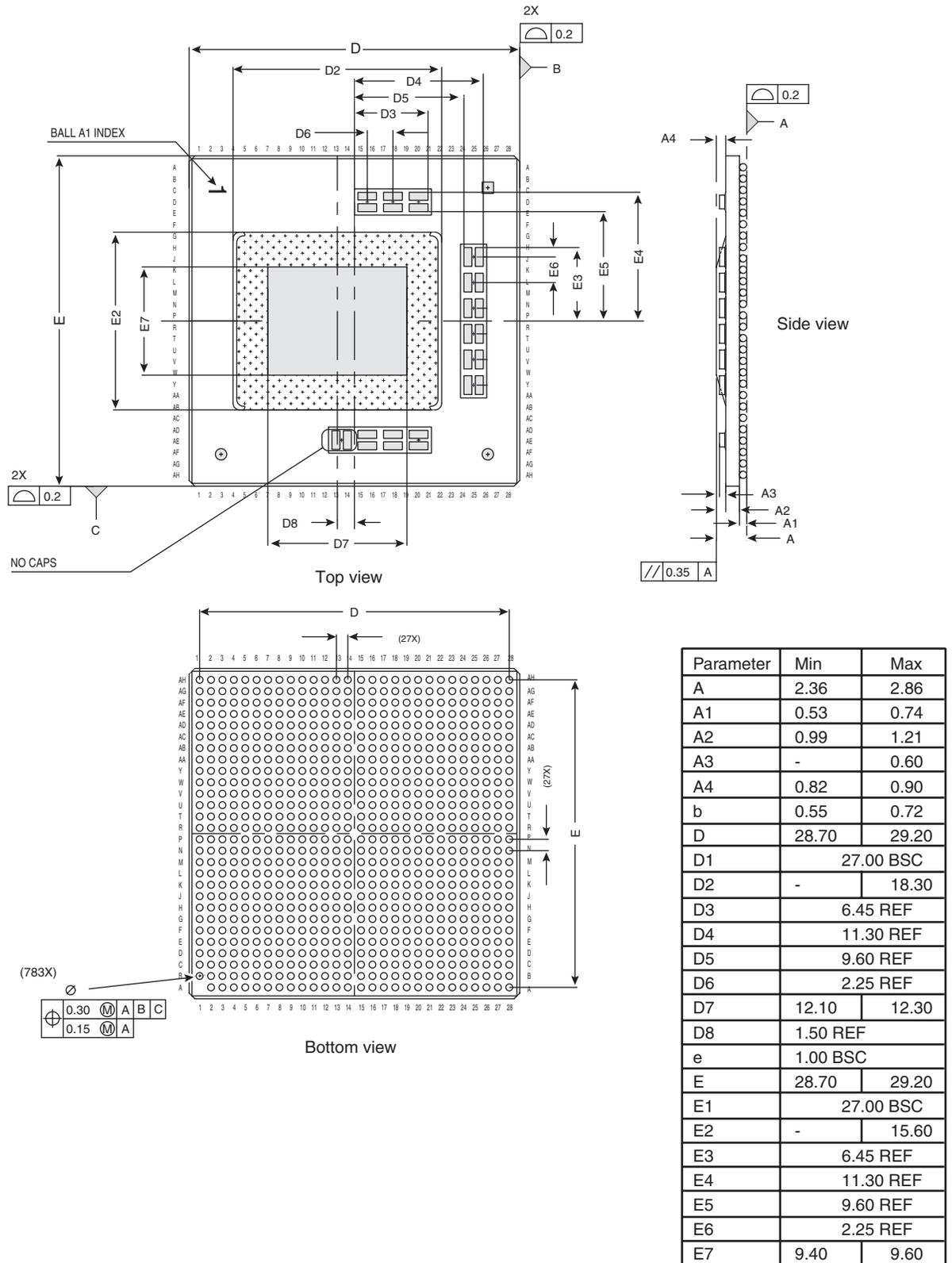
14.1 Package Parameters for the PC8540 HiTCE

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 flip chip ball grid array (HiTCE).

Die size	12.2 mm × 9.5 mm
Package outline	29 mm × 29 mm
Interconnects	783
Pitch	1 mm
Minimum module height	2.36 mm
Maximum module height	2.86 mm
Solder Balls	90 Sn/10 Pb
Ball diameter (typical)	0.6 mm

14.2 Mechanical Dimensions of the PC8540 HiTCE

shows the mechanical dimensions and bottom surface nomenclature of the PC8540, 783 HiTCE package.

Figure 14-1. Mechanical Dimensions and Bottom Surface Nomenclature of the PC8540 HiTCE

Parameter	Min	Max
A	2.36	2.86
A1	0.53	0.74
A2	0.99	1.21
A3	-	0.60
A4	0.82	0.90
b	0.55	0.72
D	28.70	29.20
D1	27.00 BSC	
D2	-	18.30
D3	6.45 REF	
D4	11.30 REF	
D5	9.60 REF	
D6	2.25 REF	
D7	12.10	12.30
D8	1.50 REF	
e	1.00 BSC	
E	28.70	29.20
E1	27.00 BSC	
E2	-	15.60
E3	6.45 REF	
E4	11.30 REF	
E5	9.60 REF	
E6	2.25 REF	
E7	9.40	9.60

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14.3   Pinout Listings

Table 14-1 provides the pin-out listing for the PC8540, 783 HiTCE package.

Table 14-1.   PC8540 Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI/PCI-X				
PCI_AD[63:0]	AA14, AB14, AC14, AD14, AE14, AF14, AG14, AH14, V15, W15, Y15, AA15, AB15, AC15, AD15, AG15, AH15, V16, W16, AB16, AC16, AD16, AE16, AF16, V17, W17, Y17, AA17, AB17, AE17, AF17, AF18, AH6, AD7, AE7, AH7, AB8, AC8, AF8, AG8, AD9, AE9, AF9, AG9, AH9, W10, Y10, AA10, AE11, AF11, AG11, AH11, V12, W12, Y12, AB12, AD12, AE12, AG12, AH12, V13, Y13, AB13, AC13	I/O	OV$_{DD}$	[17]
PCI_C_$\overline{BE}$[7:0]	AG13, AH13, V14, W14, AH8, AB10, AD11, AC12	I/O	OV$_{DD}$	[17]
PCI_PAR	AA11	I/O	OV$_{DD}$	
PCI_PAR64	Y14	I/O	OV$_{DD}$	
$\overline{PCI\_FRAME}$	AC10	I/O	OV$_{DD}$	[2]
$\overline{PCI\_TRDY}$	AG10	I/O	OV$_{DD}$	[2]
$\overline{PCI\_IRDY}$	AD10	I/O	OV$_{DD}$	[2]
$\overline{PCI\_STOP}$	V11	I/O	OV$_{DD}$	[2]
$\overline{PCI\_DEVSEL}$	AH10	I/O	OV$_{DD}$	[2]
PCI_IDSEL	AA9	I	OV$_{DD}$	
$\overline{PCI\_REQ64}$	AE13	I/O	OV$_{DD}$	[5][10]
$\overline{PCI\_ACK64}$	AD13	I/O	OV$_{DD}$	[2]
$\overline{PCI\_PERR}$	W11	I/O	OV$_{DD}$	[2]
$\overline{PCI\_SERR}$	Y11	I/O	OV$_{DD}$	[2][4]
$\overline{PCI\_REQ0}$	AF5	I/O	OV$_{DD}$	
$\overline{PCI\_REQ}$[1:4]	AF3, AE4, AG4, AE5	I	OV$_{DD}$	
$\overline{PCI\_GNT}$[0]	AE6	I/O	OV$_{DD}$	
$\overline{PCI\_GNT}$[1:4]	AG5, AH5, AF6, AG6	O	OV$_{DD}$	[5][9]
DDR SDRAM Memory Interface				
MDQ[0:63]	M26, L27, L22, K24, M24, M23, K27, K26, K22, J28, F26, E27, J26, J23, H26, G26, C26, E25, C24, E23, D26, C25, A24, D23, B23, F22, J21, G21, G22, D22, H21, E21, N18, J18, D18, L17, M18, L18, C18, A18, K17, K16, C16, B16, G17, L16, A16, L15, G15, E15, C14, K13, C15, D15, E14, D14, D13, E13, D12, A11, F13, H13, A13, B12	I/O	GV$_{DD}$	
MECC[0:7]	N20, M20, L19, E19, C21, A21, G19, A19	I/O	GV$_{DD}$	
MDM[0:8]	L24, H28, F24, L21, E18, E16, G14, B13, M19	O	GV$_{DD}$	
MDQS[0:8]	L26, J25, D25, A22, H18, F16, F14, C13, C20	I/O	GV$_{DD}$	
MBA[0:1]	B18, B19	O	GV$_{DD}$	

Table 14-1. PC8540 Pinout Listing (Continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MA[0:14]	N19, B21, F21, K21, M21, C23, A23, B24, H23, G24, K19, B25, D27, J14, J13	O	GV_{DD}	
$\overline{MWE}$	D17	O	GV_{DD}	
$\overline{MRAS}$	F17	O	GV_{DD}	
$\overline{MCAS}$	J16	O	GV_{DD}	
$\overline{MCS}$[0:3]	H16, G16, J15, H15	O	GV_{DD}	
MCKE[0:1]	E26, E28	O	GV_{DD}	(11)
MCK[0:5]	J20, H25, A15, D20, F28, K14	O	GV_{DD}	
$\overline{MCK}$[0:5]	F20, G27, B15, E20, F27, L14	O	GV_{DD}	
MSYNC_IN	M28	I	GV_{DD}	
MSYNC_OUT	N28	O	GV_{DD}	
Local Bus Controller Interface				
LA[27]	U18	O	OV_{DD}	(5)(9)
LA[28:31]	T18, T19, T20, T21	O	OV_{DD}	(7)(9)
LAD[0:31]	AD26, AD27, AD28, AC26, AC27, AC28, AA22, AA23, AA26, Y21, Y22, Y26, W20, W22, W26, V19, T22, R24, R23, R22, R21, R18, P26, P25, P20, P19, P18, N22, N23, N24, N25, N26	I/O	OV_{DD}	
LALE	V21	O	OV_{DD}	(8)(9)
LBCTL	V20	O	OV_{DD}	(9)
LCKE	U23	O	OV_{DD}	
LCLK[0:2]	U27, U28, V18	O	OV_{DD}	
$\overline{LCS}$[0:4]	Y27, Y28, W27, W28, R27	O	OV_{DD}	(18)
$\overline{LCS5}$/$\overline{DMA\_DREQ2}$	R28	I/O	OV_{DD}	(1)
$\overline{LCS6}$/$\overline{DMA\_DACK2}$	P27	O	OV_{DD}	(1)
$\overline{LCS7}$/$\overline{DMA\_DDONE2}$	P28	O	OV_{DD}	(1)
LDP[0:3]	AA27, AA28, T26, P21	I/O	OV_{DD}	
LGPL0/LSDA10	U19	O	OV_{DD}	(5)(9)
LGPL1/$\overline{LSDWE}$	U22	O	OV_{DD}	(5)(9)
LGPL2/$\overline{LOE}$/$\overline{LSDRAS}$	V28	O	OV_{DD}	(8)(9)
LGPL3/$\overline{LSDCAS}$	V27	O	OV_{DD}	(5)(9)
LGPL4/$\overline{LGTA}$/LUPWAITLPBSE	V23	I/O	OV_{DD}	(22)
LGPL5	V22	O	OV_{DD}	(5)(9)
LSYNC_IN	T27	I	OV_{DD}	
LSYNC_OUT	T28	O	OV_{DD}	

Table 14-1. PC8540 Pinout Listing (Continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{LWE}$[0:1]/LSDDQM[0:1]/$\overline{LBS}$[0:1]	AB28, AB27	O	OV$_{DD}$	(1)(5)(9)
$\overline{LWE}$[2:3]/LSDDQM[2:3]$\overline{LBS}$[2:3]	T23, P24	O	OV$_{DD}$	(1)(5)(9)
DMA				
$\overline{DMA\_DREQ}$[0:1]	H5, G4	I	OV$_{DD}$	
$\overline{DMA\_DACK}$[0:1]	H6, G5	O	OV$_{DD}$	
$\overline{DMA\_DDONE}$[0:1]	H7, G6	O	OV$_{DD}$	
DUART				
UART_SIN[0:1]	AE2, AD5	I	OV$_{DD}$	
UART_SOUT[0:1]	AE3, AD2	O	OV$_{DD}$	
$\overline{UART\_CTS}$[0:1]	U9, U7	I	OV$_{DD}$	
$\overline{UART\_RTS}$[0:1]	AD6, AD1	O	OV$_{DD}$	
Programmable Interrupt Control				
$\overline{MCP}$	AG17	I	OV$_{DD}$	
$\overline{UDE}$	AG16	I	OV$_{DD}$	
IRQ[0:7]	AA18, Y18, AB18, AG24, AA21, Y19, AA19, AG25	I	OV$_{DD}$	
IRQ8	AB20	I	OV$_{DD}$	(9)
IRQ9/$\overline{DMA\_DREQ3}$	Y20	I	OV$_{DD}$	(1)
IRQ10/$\overline{DMA\_DACK3}$	AF26	I/O	OV$_{DD}$	(1)
IRQ11/$\overline{DMA\_DDONE3}$	AH24	I/O	OV$_{DD}$	(1)
$\overline{IRQ\_OUT}$	AB21	O	OV$_{DD}$	(2)(4)
Ethernet Management Interface				
EC_MDC	F1	O	OV$_{DD}$	(5)(9)
EC_MDIO	E1	I/O	OV$_{DD}$	
Gigabit Reference Clock				
EC_GTX_CLK125	E2	I	LV$_{DD}$	
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_TXD[7:4]	A6, F7, D7, C7	O	LV$_{DD}$	(5)(9)
TSEC1_TXD[3:0]	B7, A7, G8, E8	O	LV$_{DD}$	(9)(19)
TSEC1_TX_EN	C8	O	LV$_{DD}$	(11)
TSEC1_TX_ER	B8	O	LV$_{DD}$	
TSEC1_TX_CLK	C6	I	LV$_{DD}$	
TSEC1_GTX_CLK	B6	O	LV$_{DD}$	(18)
TSEC1_CRS	C3	I	LV$_{DD}$	

PC8540 [Preliminary]

Table 14-1. PC8540 Pinout Listing (Continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_COL	G7	I	LV$_{DD}$	
TSEC1_RXD[7:0]	D4, B4, D3, D5, B5, A5, F6, E6	I	LV$_{DD}$	
TSEC1_RX_DV	D2	I	LV$_{DD}$	
TSEC1_RX_ER	E5	I	LV$_{DD}$	
TSEC1_RX_CLK	D6	I	LV$_{DD}$	
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_TXD[7:2]	B10, A10, J10, K11,J11, H11	O	LV$_{DD}$	(5)(9)
TSEC2_TXD[1:0]	G11, E11	O	LV$_{DD}$	
TSEC2_TX_EN	B11	O	LV$_{DD}$	(11)
TSEC2_TX_ER	D11	O	LV$_{DD}$	
TSEC2_TX_CLK	D10	I	LV$_{DD}$	
TSEC2_GTX_CLK	C10	O	LV$_{DD}$	(18)
TSEC2_CRS	D9	I	LV$_{DD}$	
TSEC2_COL	F8	I	LV$_{DD}$	
TSEC2_RXD[7:0]	F9, E9, C9, B9, A9, H9, G10, F10	I	LV$_{DD}$	
TSEC2_RX_DV	H8	I	LV$_{DD}$	
TSEC2_RX_ER	A8	I	LV$_{DD}$	
TSEC2_RX_CLK	E10	I	LV$_{DD}$	
10/100 Ethernet (MII) Interface				
FEC_TXD[3:0]	M1, N1, N4, N5	O	OV$_{DD}$	
FEC_TX_EN	P11	O	OV$_{DD}$	
FEC_TX_ER	P10	O	OV$_{DD}$	
FEC_TX_CLK	V6	I	OV$_{DD}$	
FEC_CRS	N10	I	OV$_{DD}$	
FEC_COL	N11	I	OV$_{DD}$	
FEC_RXD[3:0]	N9, N8, N7, N6	I	OV$_{DD}$	
FEC_RX_DV	P8	I	OV$_{DD}$	
FEC_RX_ER	P9	I	OV$_{DD}$	
FEC_RX_CLK	V9	I	OV$_{DD}$	
RapidIO Interface				
RIO_RCLK	Y25	I	OV$_{DD}$	
$\overline{RIO\_RCLK}$	Y24	I	OV$_{DD}$	
RIO_RD[0:7]	T25, U25, V25, W25, AA25, AB25, AC25, AD25	I	OV$_{DD}$	
$\overline{RIO\_RD}$[0:7]	T24, U24, V24, W24, AA24, AB24, AC24, AD24	I	OV$_{DD}$	
RIO_RFRAME	AE27	I	OV$_{DD}$	

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Table 14-1. PC8540 Pinout Listing (Continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{RIO\_RFRAME}}$	AE26	I	OV_{DD}	
RIO_TCLK	AC20	O	OV_{DD}	(11)
$\overline{\text{RIO\_TCLK}}$	AE21	O	OV_{DD}	(11)
RIO_TD[0:7]	AE18, AC18, AD19, AE20, AD21, AE22, AC22, AD23	O	OV_{DD}	
$\overline{\text{RIO\_TD}}$[0:7]	AD18, AE19, AC19, AD20, AC21, AD22, AE23, AC23	O	OV_{DD}	
RIO_TFRAME	AE24	O	OV_{DD}	
$\overline{\text{RIO\_TFRAME}}$	AE25	O	OV_{DD}	
RIO_TX_CLK_IN	AF24	I	OV_{DD}	
$\overline{\text{RIO\_TX\_CLK\_IN}}$	AF25	I	OV_{DD}	
I²C interface				
IC_SDA	AH22	I/O	OV_{DD}	(4)(20)
IIC_SCL	AH23	I/O	OV_{DD}	(4)(20)
System Control				
$\overline{\text{HRESET}}$	AH16	I	OV_{DD}	
$\overline{\text{HRESET\_REQ}}$	AG20	O	OV_{DD}	
$\overline{\text{SRESET}}$	AF20	I	OV_{DD}	
$\overline{\text{CKSTP\_IN}}$	M11	I	OV_{DD}	
$\overline{\text{CKSTP\_OUT}}$	G1	O	OV_{DD}	(2)(4)
Debug				
TRIG_IN	N12	I	OV_{DD}	
TRIG_OUT/READY	G2	O	OV_{DD}	(6)(9)(19)
MSRCID[0:1]	J9, G3	O	OV_{DD}	(5)(6)(9)
MSRCID[2:4]	F3, F5, F2	O	OV_{DD}	(6)
MDVAL	F4	O	OV_{DD}	(6)
Clock				
SYSCLK	AH21	I	OV_{DD}	
RTC	AB23	I	OV_{DD}	
CLK_OUT	AF22	O	OV_{DD}	(11)
JTAG				
TCK	AF21	I	OV_{DD}	
TDI	AG21	I	OV_{DD}	(12)
TDO	AF19	O	OV_{DD}	(11)
TMS	AF23	I	OV_{DD}	(12)
$\overline{\text{TRST}}$	AG23	I	OV_{DD}	(12)
DFT				

Table 14-1. PC8540 Pinout Listing (Continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{LSSD\_MODE}}$	AG19	I	OV_{DD}	[21]
L1_TSTCLK	AB22	I	OV_{DD}	[21]
L2_TSTCLK	AG22	I	OV_{DD}	[21]
TEST_SEL	AH20	I	OV_{DD}	[3]
Thermal Management				
THERM0	AG2	I	–	[14]
THERM1	AH3	I	–	[14]
Power Management				
ASLEEP	AG18	I/O		[9][19]
Power and Ground Signals				
$AV_{DD}1$	AH19		Power for e500 PLL (1.2V)	$AV_{DD}1$	
$AV_{DD}2$	AH18		Power for CCB PLL (1.2V)	$AV_{DD}2$	
GND	A12, A17, B3, B14, B20, B26, B27, C2, C4, C11,C17, C19, C22, C27, D8, E3, E12, E24, F11, F18, F23, G9, G12, G25, H4, H12, H14, H17, H20, H22, H27, J19, J24, K5, K9, K18, K23, K28, L6, L20, L25, M4, M12, M14, M16, M22, M27, N2, N13, N15, N17, P12, P14, P16, P23, R13, R15, R17, R20, R26, T3, T8, T10, T12, T14, T16, U6, U13, U15, U16, U17, U21, V7, V10, V26, W5, W18, W23, Y8, Y16, AA6, AA13, AB4, AB11, AB19, AC6, AC9, AD3, AD8, AD17, AF2, AF4, AF10, AF13, AF15, AF27, AG3, AG7, AG26	–	–	
GV_{DD}	A14, A20, A25, A26, A27, A28, B17, B22, B28, C12, C28, D16, D19, D21, D24, D28, E17, E22, F12, F15, F19, F25, G13, G18, G20, G23, G28, H19, H24, J12, J17, J22, J27, K15, K20, K25, L13, L23, L28, M25, N21	Power for DDR DRAM I/O Voltage (2.5V)	GV_{DD}	
LV_{DD}	A4, C5, E7, H10	Reference Voltage; Three-Speed Ethernet I/O (2.5V, 3.3V)	LV_{DD}	
MV_{REF}	N27	Reference Voltage Signal; DDR	MV_{REF}	

Table 14-1. PC8540 Pinout Listing (Continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
No Connects	AH26, AH27, AH28, AG28, AF28, AE28, AH1, AG1, AH2, B1, B2, A2, A3, AH25, H1, H2, J1, J2, J3, J4, J5, J6, J7, J8, K8, K7, K6, K3, K2, K1, L1, L2, L3, L4, L5, L8, L9, L10, L11, M10, M9, M8, M7, M6, M3, M2, P7, P6, P5, P4, P3, P2, P1, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, T9, T6, T5, T4, T1, U1, U2, U3, U4, U8, U10, V5, V4, V3, V2, V1, W1, W2, W3, W6, W7, W8, W9, Y1, Y2, Y3, Y4, Y5, Y6, Y9, AA8, AA7, AA4, AA3, AA2, AA1, AB1, AB2, AB3, AB5, AB6, AC7, AC4, AC3, AC2, AC1	–	–	(16)
OV$_{DD}$	D1, E4, H3, K4, K10, L7, M5, N3, P22, R19, R25, T2, T7, U5, U20, U26, V8, W4, W13, W19, W21, Y7, Y23, AA5, AA12, AA16, AA20, AB7, AB9, AB26, AC5, AC11, AC17, AD4, AE1, AE8, AE10, AE15, AF7, AF12, AG27, AH4	PCI/PCI-X, RapidIO, 10/100 Ethernet, and other Standard (3.3V)	OV$_{DD}$	
RESERVED	C1, T11, U11, AF1			(15)
SENSEVDD	L12	Power for Core (1.2V)	V$_{DD}$	(13)
SENSEVSS	K12			(13)
V$_{DD}$	M13, M15, M17, N14, N16, P13, P15, P17, R12, R14, R16, T13, T15, T17, U12, U14, AH17	Power for Core (1.2V)	V$_{DD}$	

Notes: 1. All multiplexed signals are listed only once and do not re-occur. For example, $\overline{LCS5}/\overline{DMA\_REQ2}$ is listed only once in the Local Bus Controller Interface section, and is not mentioned in the DMA section even though the pin also functions as $\overline{DMA\_REQ2}$.

2. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV$_{DD}$.

3. This pin must always be tied to GND.

4. This pin is an open drain signal.

5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the PC8540 is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ pull-down resistor. If an external device connected to this pin might pull it down during reset, then a pull-up or active driver is needed if the signal is intended to be high during reset.

6. Treat these pins as no connects (NC) unless using debug address functionality.

7. The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7 kΩ pull-up or pull-down resistors. See Section 15.2 "Platform/System PLL Ratio" on page 72.

8. The value of LALE and LGPL2 at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7 kΩ pull-up or pull-down resistors. See the Section 15.3 "e500 Core PLL Ratio" on page 72.

9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.

10. This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. Refer to the *PCI Specification*.

11. This output is actively driven during reset rather than being three-stated during reset.

12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.

13. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.

14. Internal thermally sensitive resistor.

15. No connections should be made to these pins.

16. These pins are not connected for any functional use.

17. PCI specifications recommend that a weak pull-up resistor (2–10 kΩ) be placed on the higher order pins to OV_{DD} when using 64-bit buffer mode (pins PCI_AD[63:32] and PCI_C_BE[7:4]).

18. Note that these signals are POR configurations for Rev. 1.x and notes 5 and 9 apply to these signals in Rev. 1.x but not in later revisions.

19. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a logic –1 state during reset.

20. Recommend a pull-up resistor (~1 kΩ) b placed on this pin to OV_{DD}.

21. These are test signals for factory use only and must be pulled up (100Ω - 1 kΩ) to OV_{DD} for normal machine operation.

22. If this signal is used as both an input and an output, a weak pull-up (~10 kΩ) is required on this pin.

15. Clocking

This section describes the PLL configuration of the PC8540. Note that the platform clock is identical to the CCB clock.

15.1 Clock Ranges

Table 15-1 provides the clocking specifications for the processor core and Table 15-2 provides the clocking specifications for the memory bus.

Table 15-1. Processor Core Clocking Specifications

| Characteristic | Maximum Processor Core Frequency | | | | | | Unit | Notes |
| | 667 MHz | | 833 MHz | | 1 GHz | | | |
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	400	667	400	833	400	1000	MHz	[1][2][3]

Notes: 1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2 "Platform/System PLL Ratio" on page 72 and Section 15.3 "e500 Core PLL Ratio" on page 72, for ratio settings.

2. The minimum e500 core frequency is based on the minimum platform frequency of 200 MHz.

3. The 1 GHz core frequency is based on a 1.3V V_{DD} supply voltage

Table 15-2. Memory Bus Clocking Specifications

| Characteristic | Maximum Processor Core Frequency | | | | | | Unit | Notes |
| | 667 MHz | | 833 MHz | | 1 GHz | | | |
	Min	Max	Min	Max	Min	Max		
Memory bus frequency	100	166	100	166	100	166	MHz	[1][2][3]

Notes: 1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 15.2 "Platform/System PLL Ratio" on page 72 and Section 15.3 "e500 Core PLL Ratio" on page 72, for ratio settings.

2. The memory bus speed is half of the DDR data rate, hence, half of the platform clock frequency.

3. The 1 GHz core frequency is based on a 1.3V V_{DD} supply voltage.

15.2 Platform/System PLL Ratio

The platform clock is the clock that drives the L2 cache, the DDR SDRAM data rate, and the e500 core complex bus (CCB), and is also called the CCB clock. The values are determined by the binary value on LA[28:31] at power up, as shown in Table 15-3.

There is no default for this PLL ratio; these signals must be pulled to the desired values.

Table 15-3. CCB Clock Ratio

Binary Value of LA[28:31] Signals	Ratio Description
0000	16:1 ratio CCB clock: SYSCLK (PCI bus)
0001	Reserved
0010	2:1 ratio CCB clock: SYSCLK (PCI bus)
0011	3:1 ratio CCB clock: SYSCLK (PCI bus)
0100	4:1 ratio CCB clock: SYSCLK (PCI bus)
0101	5:1 ratio CCB clock: SYSCLK (PCI bus)
0110	6:1 ratio CCB clock: SYSCLK (PCI bus)
0111	Reserved
1000	8:1 ratio CCB clock: SYSCLK (PCI bus)
1001	9:1 ratio CCB clock: SYSCLK (PCI bus)
1010	10:1 ratio CCB clock: SYSCLK (PCI bus)
1011	Reserved
1100	12:1 ratio CCB clock: SYSCLK (PCI bus)
1101	Reserved
1110	Reserved
1111	Reserved

15.3 e500 Core PLL Ratio

Table 15-4. e500 Core to CCB Ratio

Binary Value of LALE, LGPL2 Signals	Ratio Description
00	2:1 e500 core:CCB
01	5:2 e500 core:CCB
10	3:1 e500 core:CCB
11	7:2 e500 core:CCB

15.4 Frequency Options

Table 15-5 shows the expected frequency values for the platform frequency when using a CCB to SYSCLK ratio in comparison to the memory bus speed.

Table 15-5. Frequency Options with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)								
	16.67	25	33.33	41.63	66.67	83	100	111	133.33
	Platform/CCB Frequency (MHz)								
2							200	222	267
3					200	250	300	333	
4					267	333			
5				208	333				
6			200	250					
8		200	267	333					
9		225	300						
10		250	333						
12	200	300							
16	267								

16. Thermal

This section describes the thermal specifications of the PC8540.

16.1 Thermal Characteristics

Table 16-1 provides the package thermal characteristics for the PC8540.

Table 16-1. PC8540 CBGA783 HiTCE Thermal Simulation

Characteristic	Value	Unit
Thermal resistance junction to bottom of balls	3.4	°C/W
Thermal resistance junction to board, Jedec JESD51-8	7.2	°C/W
Thermal resistance junction to ambient, Jedec JESD51-2	16.3	°C/W
Thermal resistance junction to top of die: - directly on Silicon backside (not advised on the field - with thermal interface	0.13 0.81	°C/W

16.1.1 Internal Package Conduction Resistance

For the packaging technology, shown in Table 17-1 on page 78, the intrinsic internal conduction thermal resistance paths are as follows:

• The die junction-to-case thermal resistance

• The die junction-to-board thermal resistance

Figure 17-2 on page 78 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Figure 16-1. Package with Heat Sink Mounted to a Printed-Circuit Board
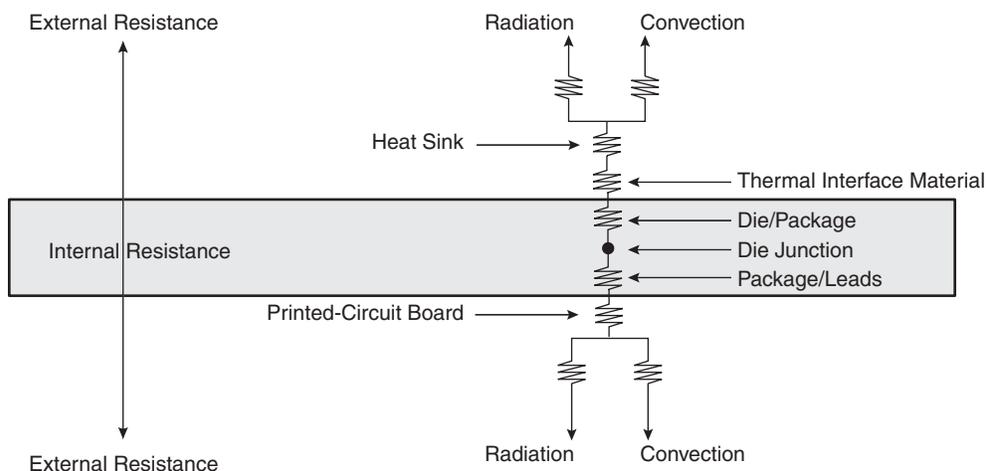
Note the internal versus external package resistance.

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the lid, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

16.1.2   Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 17-3 on page 81 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 16-1). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

When removing the heat sink for re-work, it is preferable to slide the heat sink off slowly until the thermal interface material loses its grip. If the support fixture around the package prevents sliding off the heat sink, the heat sink should be slowly removed. Heating the heat sink to 40-50×C with an air gun can soften the interface material and make the removal easier. The use of an adhesive for heat sink attach is not recommended.

Figure 16-2. Thermal Performance of Select Thermal Interface Materials
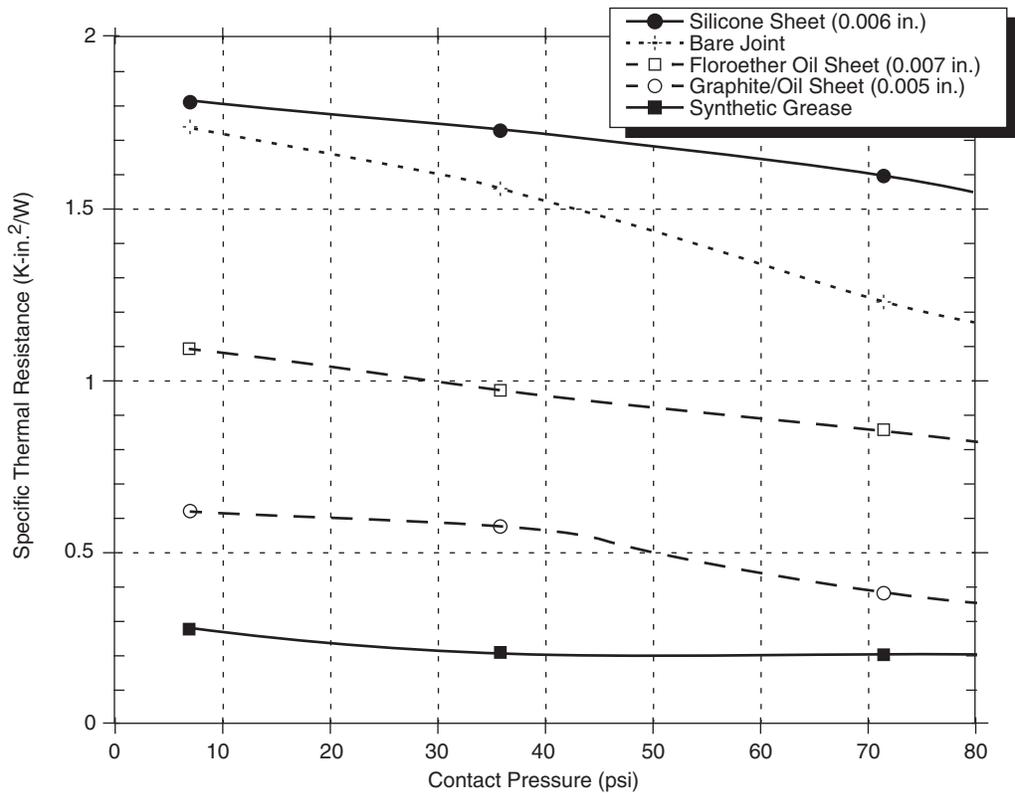
Figure 16-3. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity
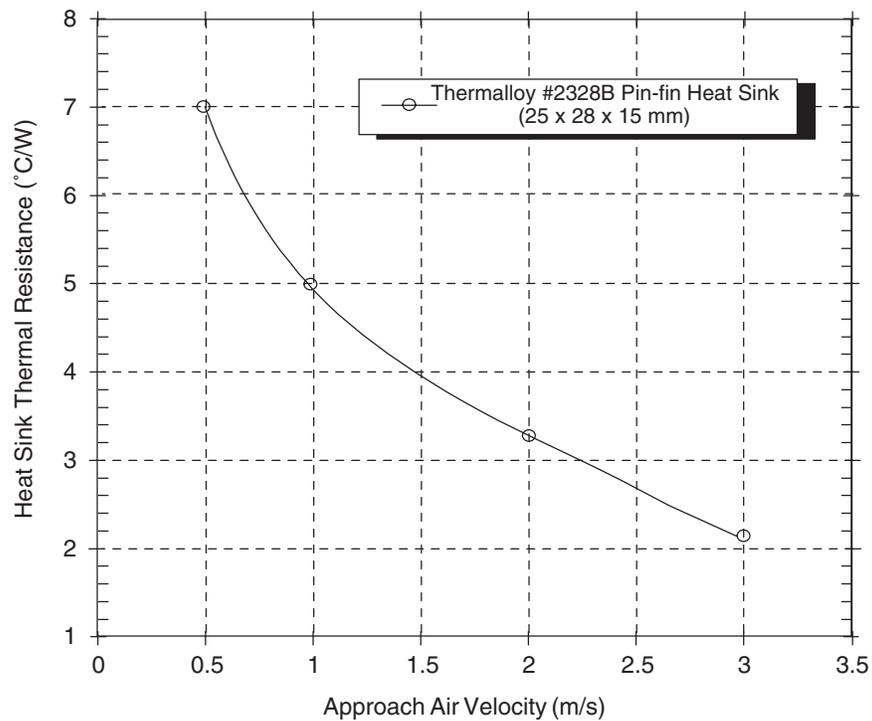
17. System Design Information

This section provides electrical and thermal design recommendations for successful application of the PC8540.

17.1 System Clocking

The PC8540includes two PLLs.

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 15.2 "Platform/System PLL Ratio" on page 72.

2. The e500 Core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 15.3 "e500 Core PLL Ratio" on page 72.

17.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}1$ and $AV_{DD}2$, respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide three independent filter circuits as illustrated in Figure 17-1, one to each of the three AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 783 HiTCE footprint, without the inductance of vias.

Figure 17-1 shows the PLL power supply filter circuit.

Figure 17-1. PLL Power Supply Filter Circuit
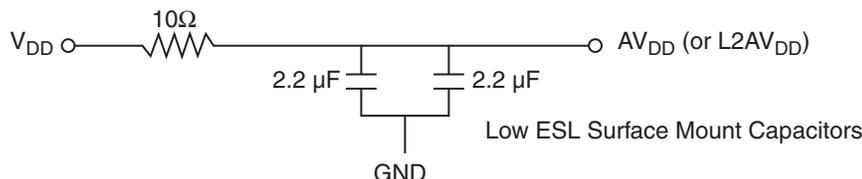
17.3   Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the PC8540 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PC8540 system, and the PC8540 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pins of the PC8540. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes. In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors: 100-330 µF (AVX TPS tantalum or Sanyo OSCON).

17.4   Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}, GV_{DD}, or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and GND pins of the PC8540.

17.5   Output Buffer DC Impedance

The PC8540 drivers are characterized over process, voltage, and temperature. There are two driver types: a push-pull single-ended driver (open drain for I^{2}C) for all buses except RapidIO, and a current-steering differential driver for the RapidIO port. To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 17-2). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Figure 17-2. Driver Impedance Measurement
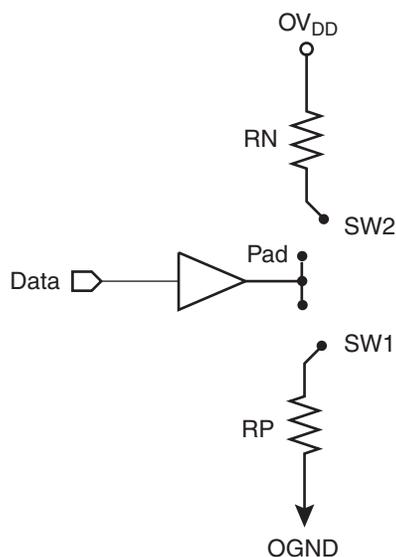
The output impedance of the RapidIO port drivers targets 200Ω differential resistance. The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 17-1 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 17-1. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI/PCI-X	DDR DRAM	RapidIO	Symbol	Unit
R_N	43 Target	25 Target	20 Target	NA	Z_0	W
R_P	43 Target	25 Target	20 Target	NA	Z_0	W
Differential	NA	NA	NA	200 Target	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 2-1 on page 7, T = 105°C

17.6 Configuration Pin Muxing

The PC8540 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7 kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform/system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

17.7 Pull-Up Resistor Requirements

The PC8540 requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including EPIC interrupt pins. I^{2}C open drain type pins should be pulled up with ~1 kΩ resistors.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 17-3 on page 81. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

TSEC1_TXD[3:0] must not be pulled low during reset. Some PHY chips have internal pulldowns that could cause this to happen. If such PHY chips are used, then a pullup must be placed on these signals strong enough to restore these signals to a logical 1 during reset.

Three test pins also require pull-up resistors (100Ω - 1 kΩ). These pins are L1_TSTCLK, L2_TSTCLK, and $\overline{\text{LSSD\_MODE}}$. These signals are for factory use only and must be pulled up to OV$_{DD}$ for normal machine operation.

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

17.8   JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. The PC8540 requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems will assert $\overline{\text{TRST}}$ during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 17-3 allows the COP to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted.

The COP header shown in Figure 17-3 adds many benefits: breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface, and can be as inexpensive as an unpopulated footprint for a header to be added when needed.The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). There is no standardized way to number the COP header shown in Figure 17-3; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 17-3 is common to all known emulators.

Figure 17-3. JTAG Interface Connection

Notes: 1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented. Connect pin 5 of the COP header to OV$_{DD}$ with a 10 kΩ pull-up resistor.

2. Key location; pin 14 is not physically present on the COP header.

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18. Definitions

18.1 Life Support Applications

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. e2v customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify e2v for any damages resulting from such improper use or sale.

19. Ordering Information

xx	8540	y	xx	n	L	x
Product Code[1]	Part Identifier	Temperature Range: T_J [1]	Package[1]	Max Internal Processor Speed[1]	Plateform frequency	Revision Level[1]
PC(X)[2]	8540	M: -55˚C, +125˚C V: -40˚C, 110˚C	GH: HiTCE	833: 833 MHz	L: 333 MHz	B: rev 2.0

Notes: 1. For availability of the different versions, contact your local e2v sales office.

2. The letter X in the part number designates a "Prototype" product that has not been qualified by e2v. Reliability of a PCX part-number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.

20. Document Revision History

provides a revision history for this hardware specification.

Table 20-1.   Document Revision History

Revision Number	Date	Substantive Change(s)
B	09/2007	Name change from Atmel to e2v Ordering information update
A	09/2005	Initial revision

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