EV12AS200AZPY-EB Evaluation Board

User Guide

1133BX–BDC–12/14

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Section 1
Introduction

1.1 Scope

The EV12AS200AZPY-EB Evaluation Kit is designed to facilitate the evaluation and characterization of the EV12AS200A 12-bit 1.5 GSps ADC in AC coupled mode.

The EV12AS200AZPY-EB Evaluation Kit includes:

- The 12-bit 1.5 GSps ADC Evaluation board including EV12AS200AZPY and µcontroller "CYPRESS" high-speed USB peripheral controller soldered.
- A CD ROM with the datasheet, present user guide and software tools necessary to use the SPI.
- A cable for connection to the mini USB port.

The user guide uses the EV12AS200AZPY-EB Evaluation Kit as an evaluation and demonstration platform and provides guidelines for its proper use.

1.2 Description

The EV12AS200AZPY-EB Evaluation board is very straightforward as it implements e2v EV12AS200A 12-bit 1.5 GSps ADC device, SMA connectors for the sampling clock, analogue inputs and reset input accesses and 2.54 mm pitch connectors compatible with high speed acquisition system probes.

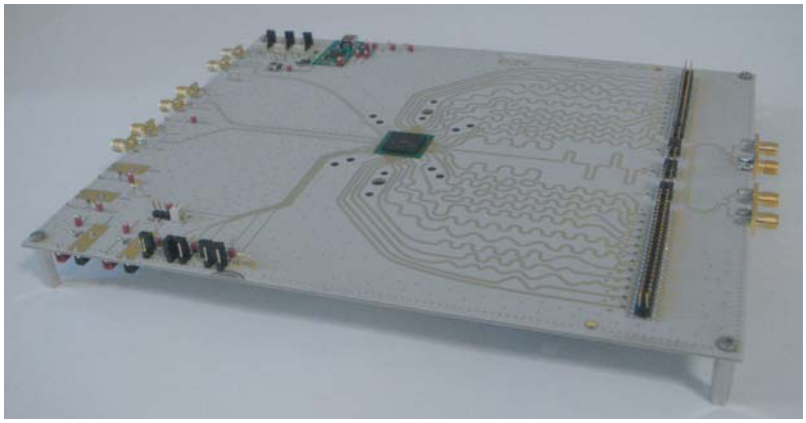
Thanks to its user-friendly interface, the EV12AS200AZPY-EB Kit enables to test all the functions of the EV12AS200AZPY 12-bit 1.5 GSps ADC.

To achieve optimal performance, the EV12AS200AZPY-EB Evaluation board was designed in a 6-metal-layer board using FR4 HTG epoxy dielectric material (200 µm, ISOLA IS410 featuring a resin content of 45%). The board implements the following devices:

- The 12-bit 1.5 GSps ADC Evaluation board with the EV12AS200AZPY ADC soldered.
- SMA connectors for CLK, CLKN, VIN, VINN, SYNC and SYNCN signals.
- SMA connectors for calibration lines.
- 2.54 mm pitch connectors for the digital outputs, compatible with high speed acquisition system probes.
- Banana jacks (2 mm) for the power supply accesses, the Die junction Temperature monitoring functions.
- Jumpers for SDAEN, SDA, RS, TM, OA, GA, Mode_n.

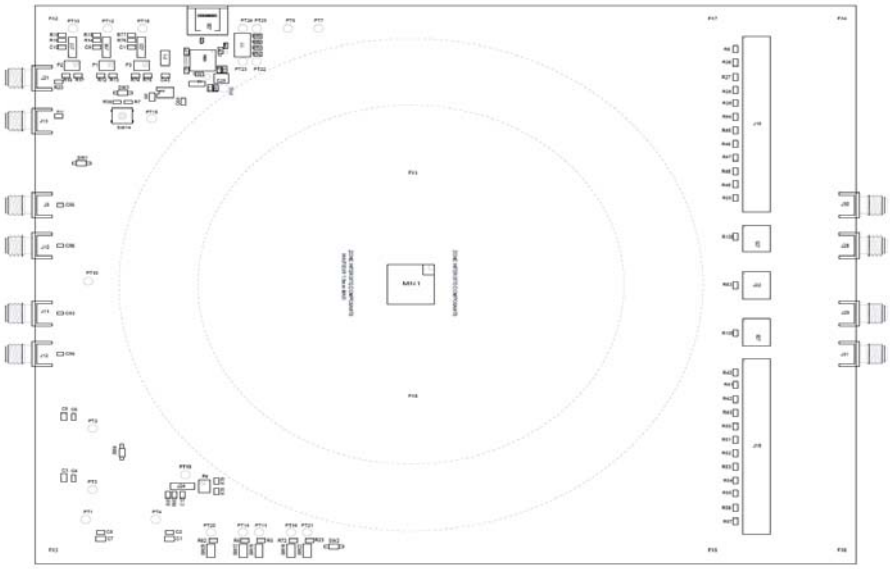
- Potentiometers for OA, GA, SDA.
- Mini USB port.

Figure 1-1. EV12AS200AZPY-EB Evaluation Board



The board dimensions are 260 mm x 210 mm.
The board comes fully assembled and tested, with the EV12AS200A installed.

Figure 1-2. EV12AS200AZPY-EB Evaluation Board Simplified Schematic



As shown in Figure 1-1, different power supplies are required:

- V_{CC5} = 5V analogue positive power supply (referenced to AGND)
- V_{CC3} = 3.3V analogue positive power supply (referenced to AGND)
- V_{CCO} = 2.5V digital output power supply (referenced to DGND)
- 3.3V board supply for control functions (referenced to DGND)
- 5V by mini USB port

Note that is also permitted to supply V_{CCO} with 3.3V in order to provide only two supplies voltages.

Section 2
Hardware Description

2.1 Board Structure

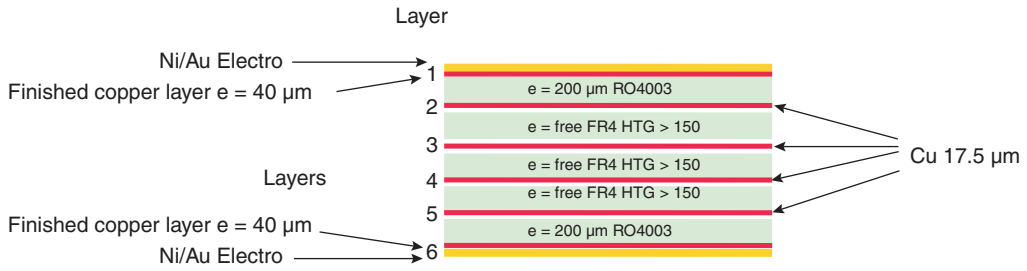
In order to achieve optimum full speed operation of the EV12AS200A 12-bit 1.5 GSps ADC, a multi-layer board structure was retained for the evaluation board. Six copper layers are used, dedicated to the signal traces, ground planes and power supply planes.

The board is made in FR4 HTG epoxy dielectric material (ISOLA IS410).

Board characteristics:

- RO4003 for the top and bottom layers, FR4 HTG for the internal layers
- Dielectric thickness: 200 µm
- Dielectric constant: 3.38
- Lands diameter: 750 µm
- GND Via/Land Diameter: 200 µm

Construction:



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The following table gives a detailed description of the board's structure.

Table 2-1. Board Layer Thickness Profile

Layer	Characteristics
Layer 1 Copper layer	Copper thickness = 40 mm (with NiAu finish) AC signals traces = 50Ω microstrip lines DC signals traces
FR4 HTG / dielectric layer	Layer thickness = 200 µm
Layer 2 Copper layer	Copper thickness = 18 µm AGND, DGND (separate planes)
FR4 HTG / dielectric layer	Layer thickness = 349 µm
Layer 3 Copper layer	Copper thickness = 18 µm Power planes = V_{CC5}, V_{CC3}, V_{CCO}, 3V3 USB
FR4 HTG / dielectric layer	Layer thickness = 350 µm
Layer 4 Copper layer	Copper thickness = 18 µm Power planes = 3V3
FR4 HTG / dielectric layer	Layer thickness = 350 µm
Layer 5 Copper layer	Copper thickness = 18 µm AGND, DGND (separate planes)
FR4 HTG / dielectric layer	Layer thickness = 200 µm
Layer 6 Copper layer	Copper thickness = 40 µm (with NiAu finish) AC signals traces = 50Ω microstrip lines DC signals traces

The board is 1.6 mm thick.

The Clock, analogue inputs, reset and ADC functions occupy the top metal layer. The digital data output signals occupy the top and bottom layers.

The Ground planes occupy layer 2 and 5.
Layer 3 and 4 are dedicated to the power supplies.

2.2 Analogue Inputs/Clock Input

The differential clock and analogue inputs are provided by SMA connectors (Reference: JOHNSON 142-0701-851-6).

Both pairs are AC coupled using 10 nF capacitors.

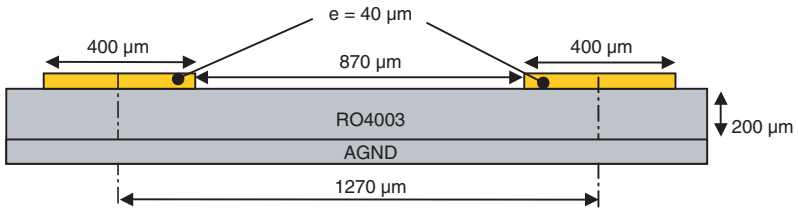
Special care was taken for the routing of the analog and clock input signals for optimum performance in the high frequency domain:

- 50Ω lines matched to ± 0.1 mm (in length) between VIN and VINN or CLK and CLKN.
- 1270 µm between two differential pairs.
- 400 µm line width.
- 40 µm thickness.
- 870 µm diameter hole in the ground layer below the VIN and VINN or CLK and CLKN ball footprints.

- In addition, the lines for VIN, VINN and CLK, CLKN are matched to one another within ±1mm.
- A clearance in the ground plane below the CLK, CLKN and VIN, VINN package lands is necessary.

Note: These values have been calculated with RO4003 dielectric material.

Figure 2-1. Board Layout for the Differential Analog and Clock Inputs with RO4003



Note: The analogue inputs and clock inputs are AC coupled with 10 nF very close to the SMA connectors.

2.3 Digital Output Data

The high speed differential output signals (digital output, clock output), are routed in parallel with 50 ohm impedance, 370 µm width and a pitch of 0.77 mm.

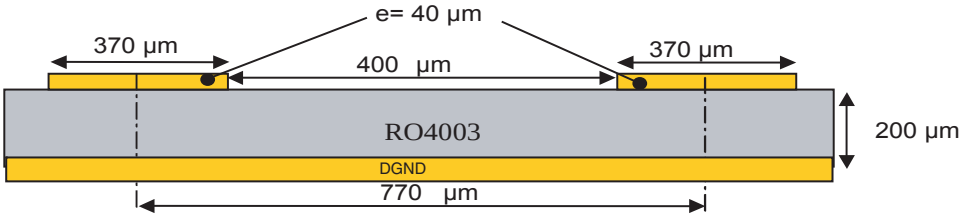
Max difference between any two signals = ±1.5mm.

Max difference between longest and shortest data per port = ±1mm.

Max difference between two signals of the same differential pair (Xi, XiN) = ±0.5mm (where X = A and B, i = 0…9).

Note: These values have been calculated with RO4003 dielectric material.

Figure 2-2. Recommended Routing on RO4003 for Digital Output Data Signals



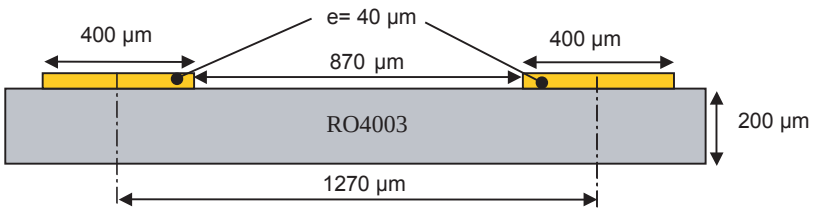
2.4 SYNC, SYNCN

A power up reset ensures that the first digitized data corresponds to the first acquisition. An external differential LVDS Reset (SYNC, SYNCN) can also be used. RES function allows changing the active edge of the RESET signal.

The differential reset inputs SYNC, SYNCN are provided by SMA connectors (Reference: VITELEC 142-0701-8511).The signals are AC coupled.

- 50Ω lines matched to ± 0.1 mm (in length) between SYNCP and SYNCN
- 1270 µm between two differential pairs
- 400 µm line width
- 40 µm thickness
- 870 µm diameter hole in the ground layer below SYNC, SYNCN ball footprints

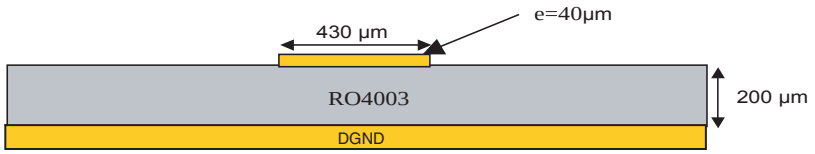
Figure 2-3. Recommended Routing on RO4003 for RSTN Signal



2.5 RS, TM, SDA, SDAEN, GA, OA, RESETN, MODE_n, Diode and CMIRef

These are "static" signals. They are routed in single-ended 50 ohm impedance.

Figure 2-4. Recommended Routing on RO4003 for static Signal



2.6 Ground Layers

There are 2 separated planes for the AGND and the DGND on the PCB. These planes must be reunited via 0Ω resistors. Only the input clock and analogue input are referenced to AGND, the other parts of the ADC are referenced to DGND.

2.7 Power Supplies

Layers 3 and 4 are dedicated to power supply planes:

V_{CC5}: ADC Analog part supply (V_{CC5} = 5V)

V_{CC3}: ADC Analogue Core and Digital parts supply (V_{CC3} = 3.3V)

V_{CCO}: ADC Output buffers supply (V_{CCO} = 2.5V)

3.3V: external reference for GA, OA and SDA commands.

5V by mini USB port: SPI.

The supply traces are low impedance and are surrounded by two ground planes (layer 2 and 5).

Each incoming power supply is bypassed at the banana jack by a 1 µF Tantalum capacitor in parallel with a 100 nF chip capacitor.

Each power supply is decoupled as close as possible to the EV12AS200AZPY device by 10 nF in parallel with 100 pF surface mount chip capacitors.

Note: The decoupling capacitors are superimposed with the 100 pF capacitor mounted first.

Section 3

Operating Characteristics

3.1 Introduction

This section describes a typical configuration for operating the evaluation board of the EV12AS200AZPY 12-bit 1.5 GSps ADC.

The analogue input signals and the sampling clock signal should be accessed in a differential fashion. Band pass filters should also be used to optimize the performance of the ADC both on the analog input and on the clock.

It is necessary to use a very low jitter source for the clock signal (better than 100fsrms jitter).

Note: 1. The analogue inputs and clock are AC coupled on the board.

3.2 Operating Procedure

1. Begin by installed **Setup_EV12AS200A_1.0.5.exe** file on your system.
2. Connect mini USB port. (red led switch on)
3. Connect the power supplies and ground accesses through the dedicated banana jacks. V_{CC5} = 5.2V, V_{CC3} = 3.3V, V_{CCO} = 2.5V, board supply = 3.3V.
4. Connect the clock input signals.
   The clock input level is typically +4dBm on ADC input (if you use balun or filter take into account the losses in the chain of measure).
   The clock frequency should be set to 1.5 GHz.
5. Connect the analogue input signals (the board has been designed to allow only AC coupled analogue inputs).
   Use a low-phase noise High Frequency generator as well as a band pass filter to optimize the analogue input performance.
   The analogue input Full Scale is 500mV peak-to-peak around zero (analogue input providing the Input common mode).
6. Connect the high speed acquisition system probes to the output connectors.
   The digital data are differentially terminated on-board (100Ω) however, they can be probed either in differential.
7. Switch on the ADC power supplies (recommended power up sequence: simultaneous or in the following order: V_{CC3} = 3.3V, V_{CC5} = 5.2V, V_{CCO} = 2.5V, board supply 3. 3V.
8. Turn on the RF clock generator.
9. Turn on the RF signal generator.

The EV12AS200AZPY-EB evaluation board is now ready for operation.

3.3 Electrical Characteristics

Values in the table below are given for information only. For more accurate values, please refer to the device datasheet.

Table 3-1. Recommended Conditions of Use

Parameter	Symbol	Comments	Typ	Unit
Power supplies(1)(2)	V_{CC5}		5.0	V
	V_{CC3}		3.3	V
	V_{CC0}		2.5	V
Differential analog input voltage (Full Scale)	$V_{IN} - V_{INN}$	100Ω differential	500	mVpp
Clock input power level (Ground common mode)	P_{CLK} P_{CLKN}	100Ω differential input	7	dBm
Operating Temperature Range	T_{case} $T_{junction}$	Commercial “C” grade Industrial “V” grade	Tc > 0 < Tj < 90 Tc > –40 < Tj < 110	°C
Storage Temperature	Tstg		–65 to 150	°C

Notes: 1. No specific power supplies sequencing is required; however to benefit from the internal reset at power up, V_{CC3} should be applied before V_{CC5}
2. V_{CCO} could be merged to V_{CC3} to use the device using only 2 power supplies.

Table 3-2. Electrical characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
ADC RESOLUTION			12		bit	
POWER REQUIREMENTS						
Power Supply voltage						
- Analogue	VCC5	4.75	5.0	5.25	V	1
- Analogue Core and Digital	VCC3	3.15	3.3	3.45	V	1
- Output buffers (2.5V configuration)	VCCO	2.4	2.5	2.6	V	1
- Output buffers (3V configuration)	VCCO	3.15	3.3	3.45	V	1
Power Supply current in 1:1 DEMUX						
- Analogue	I_VCC5		170	190	mA	1
- Analogue Core and Digital	I_VCC3		535	600	mA	1
- Output buffers	I_VCCO		50	70	mA	1
Power Supply current in 1:2 DEMUX Ratio						
- Analogue	I_VCC5		170	190	mA	1
- Analogue Core and Digital	I_VCC3		540	600	mA	1
- Output buffers	I_VCCO		90	110	mA	1
Power dissipation DMUX1:1						
- 1:1 Ratio with standard LVDS output swing, 750 Msps output rate **(Vcco = 2.5V)**	P_D		2.75	3.0		1
- 1:1 Ratio with standard LVDS output swing, 750 Msps output rate **(Vcco = 3.3V)**	P_D		2.9	3.15		4

Table 3-2. Electrical characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
Power dissipation DMUX1:2					W	
- 1:2 Ratio with standard LVDS output swing, 1500 Msps output rate (Vcco = 2.5V)	P_D		2.85	3.10		1
- 1:2 Ratio with standard LVDS output swing, 1500 Msps output rate (Vcco = 3.3V)	P_D		3.0	3.25		1
LVDS Data and Data Ready Outputs						
Logic compatibility		LVDS differential				
Output Common Mode (1)	V_{OCM}	1.125	1.25	1.375	V	1
Differential output (1)	V_{ODIFF}	250	350	450	mVpp	1
Output level “High” (2)	V_{OH}	1.25	–	–	V	1
Output level “Low” (2)	V_{OL}	–	–	1.25	V	1
Output current level (2)	I_O	–	–	100	µA	
Output data format		Binary				
ANALOG INPUT						
Input type		AC coupled				
Analogue input Common mode (for DC coupled input)(5)			3.0			
Full scale input voltage range (differential mode)(6)	V_{IN} V_{INN}	–125 –125		+125 +125	mVp mVp	
Full scale analog input power level	P_{IN}		–5		dBm	
Analog input capacitance (die only)	C_{IN}		0.3		pF	
Input leakage current (V_{IN} = V_{INN} = 0V)	I_{IN}		50		µA	
Analog Input resistance (Differential)	R_{IN}	90	100	110	Ω	
CLOCK INPUT (CLK, CLKN)						
Input type		DC or AC coupled				
Clock Input Common Mode (for DC coupled clock)	V_{ICM}		2.65		V	
Clock Input power level (low phase noise sinewave input) 100Ω differential	P_{CLK}	0	4	10	dBm	
Clock input swing (differential voltage) on each clock input	V_{CLK} V_{CLKN}	±447	±708	2800	mVp	
Clock input capacitance (die only)	C_{CLK}		0.3		pF	
Clock Input resistance (Differential)	R_{CLK}		100		Ω	
SYNC, SYNCN						
Logic compatibility		LVDS				
Input Common Mode	V_{ICM}	1.125	1.25	1.375	V	
Differential input	V_{IDIFF}	250	350	450	mVp	
Input level “High”	V_{IH}			1.8	V	
Input level “Low”	V_{IL}	0.7			V	

Table 3-2. Electrical characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Level
DIGITAL INPUTS (RS, DEC_n, SDAEN_n, TM_n)						
Logic low Resistor to ground Voltage level Input current	 R_{IL} V_{IL} I_{IL}	 0		 10 0.5 450	 Ω V µA	
Logic high Resistor to ground Voltage level Input current	 R_{IH} V_{IH} I_{IH}	 10 2.0		 100 150	 KΩ V µA	
OFFSET, GAIN , SAMPLING DELAY & CLOCK ADJUST SETTINGS (OA, GA, SDA)						
Min voltage for minimum Gain, Offset or SDA	Analog_min	$2*V_{cc3}/3 - 0.5$			V	
Max voltage for maximum Gain, Offset or SDA	Analog_max			$2*V_{cc3}/3 + 0.5$	V	
Input current for min setting	I_{min}			200	µA	
Input current for nominal setting	I_{nom}			50	µA	
Input current for max setting	I_{max}			200	µA	
3WSI (sclk, sld_n, mosi, reset_n, mode_n) INPUTS						
Logic compatibility		3.3V CMOS				
Low Level input voltage	V_{IL}	0		1	V	
High Level input voltage	V_{IH}	2.3		V_{cc3}	V	
Low Level input current	I_{IL}		100		µA	
High Level input current	I_{IH}		100		µA	
DC ACCURACY						
Differential Non Linearity (for information only)	I DNL I			2	LSB	1
Peak positive Integral Non Linearity (for information only)(7)	INL+		5		LSB	1
Peak negative Integral Non Linearity(7)	INL-		–5		LSB	1
Gain central value (3)	ADC_{GAIN}	0.8	1.0	1.2		1
Gain error drift versus temperature (over 15°C)				0.15	dB	4
Initial ADC offset (4)	ADC_{OFFSET}	1948	2048	2148	LSB	1

Notes:
1. Assuming 100Ω termination ASIC load
2. V_{OH} min and V_{OL} max can never be 1.25V at the same time when V_{ODIFF}min.
3. The ADC Gain center value can be tuned to 1.0 using Gain adjust function. Estimated at Fs = 1 GHz, Fin = 400 MHz
4. The ADC offset can be tuned to mid code 2048 using Offset adjust function.
5. For DC coupling application, the common mode value to apply is available as reference on the CMIREF pin.
6. Minimum input level validated is –12 dBFS.
7. INL is measured at –1dBFS

Section 4

Software Tools

4.1 Overview

The EV12AS200AZPY-EB Evaluation user interface software is a Visual C++ compiled graphical interface that does not require a licence to run on a Windows NT and Windows 2000/98/XP/Seven PC.

The software uses intuitive push-buttons and pop-up menus to write data from the hardware.

4.2 Getting Started

This section will guide you step by step through installation process of EV12AS200A application.

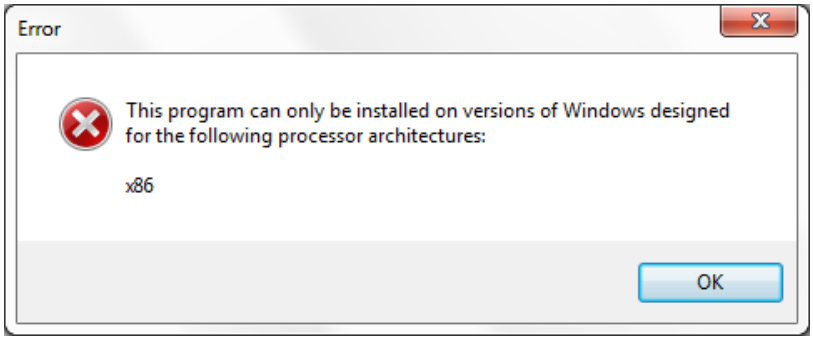
Installation process is available on Microsoft operating system from Windows 2000 to Windows Seven. Only 32bits operating system is currently supported.

Begin by locating **Setup_EV12AS200A_1.0.5.exe** file on your system, and launch it.

Setup required administrative privilege execution. If you don't have such right, please, contact your IT manager.

On recent operating system, a warning message is shown regarding higher privilege require. Answer **Yes**, otherwise setup will stop.

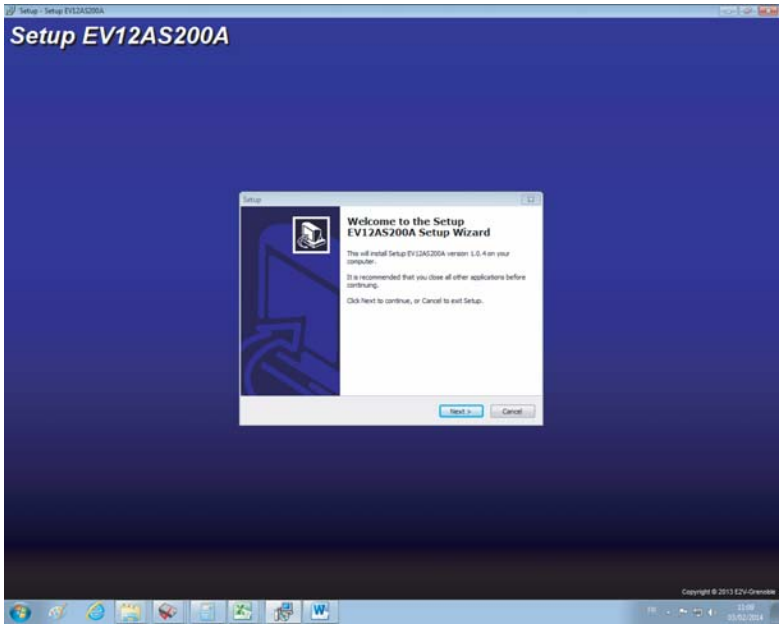
If your operating systems not 32bits, the following message will be display.



Setup process will start with this first information screen.

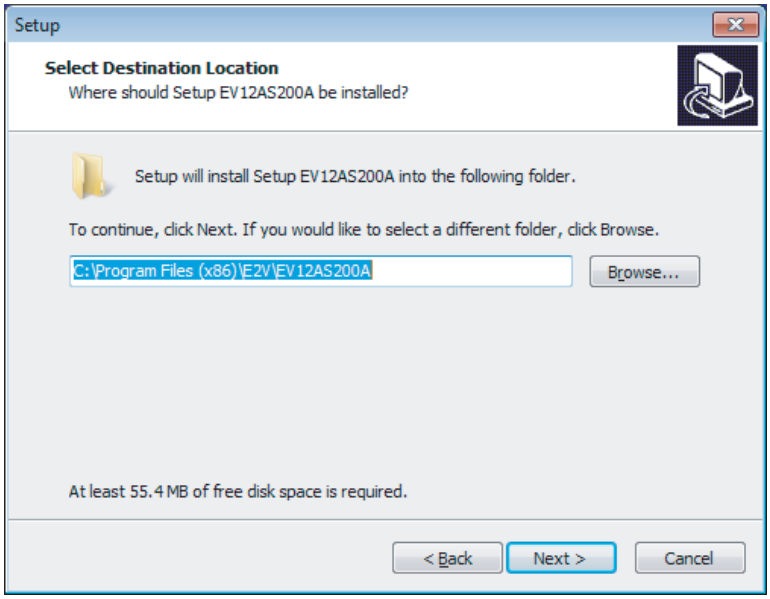
Click on **Next** to step to the next screen.

Figure 4-1. EV12AS200A Application Setup Wizard Window



This dialog displays destination directory of application. Change it to your convenience, or choose it by clicking on **Next** button.

Figure 4-2. EV12AS200A Select Destination Directory Window



Next dialog displays Start Menu entry to store application shortcut. Change it to your convenience, or choose it by clicking on **Next** button.

Figure 4-3. EV12AS200A Select Start Menu Window

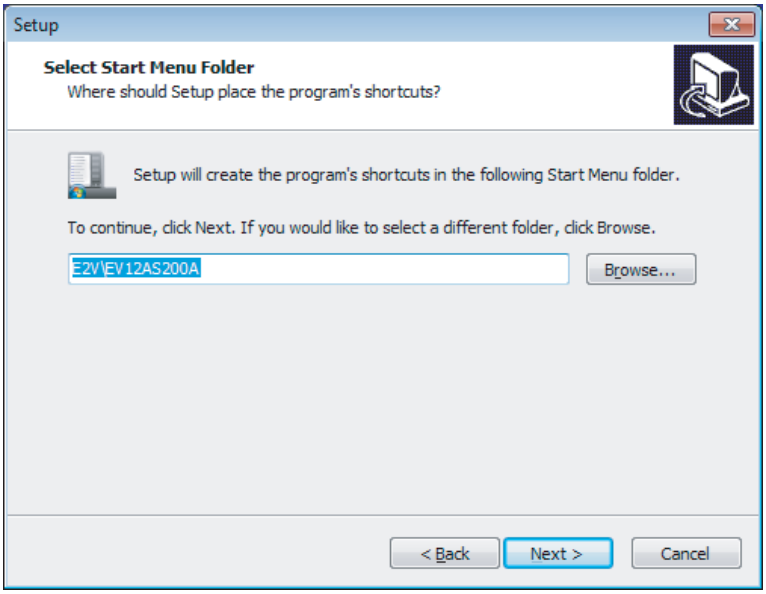


Figure 4-4. EV12AS200A Select Additional Tasks Window

Next dialog asks you if you want an application shortcut on your desktop. Change it to your convenience, or choose it by clicking on **Next** button.

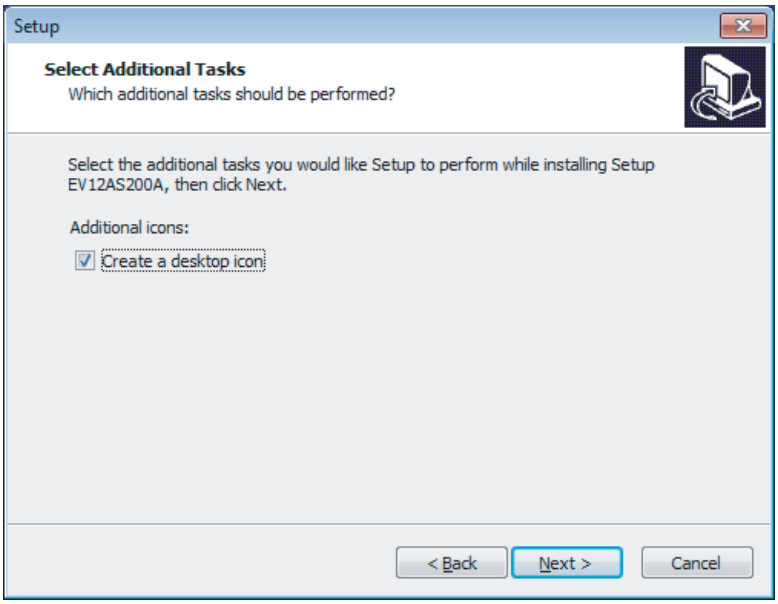
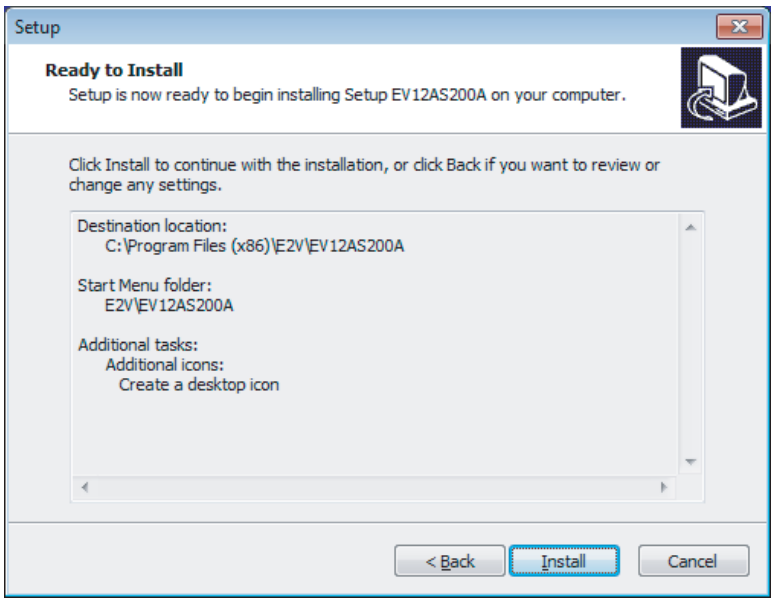


Figure 4-5. EV12AS200A Ready To Install Window

Next dialog shows a resume about operations setup will perform to complete installation. If you're agreeing, click on **Install** to start it.



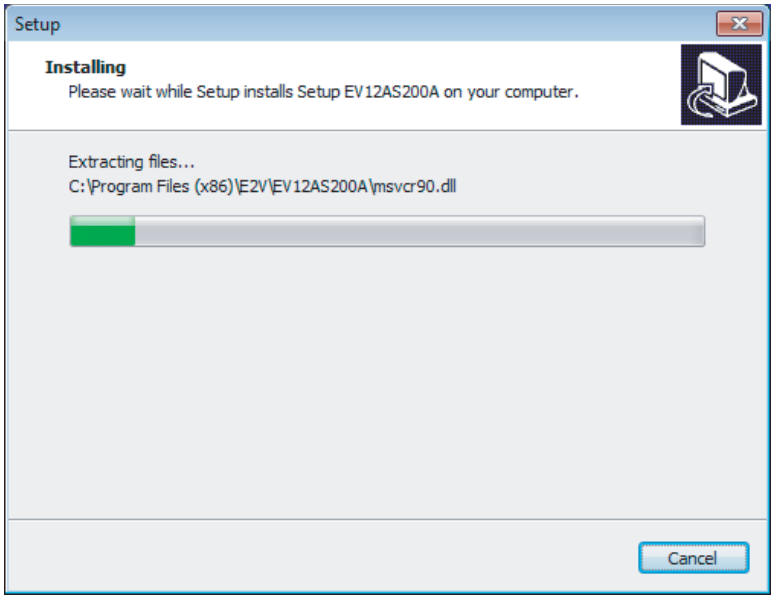
Several dialogs will be show according tasks to do.

If you agree with the install configuration, press Install button.

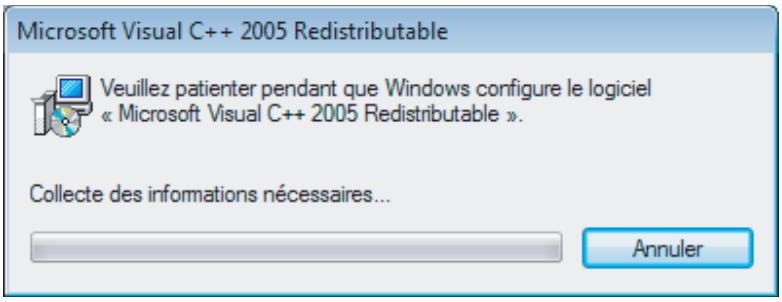
Figure 4-6. EV12AS200A Application Setup *Install* Push Button

The installation of the software is now complete.

Figure 4-7. EV12AS200A Setup Window



Microsoft Visual C++ 2005 Redistributable may take times to complete. Please, be patient.

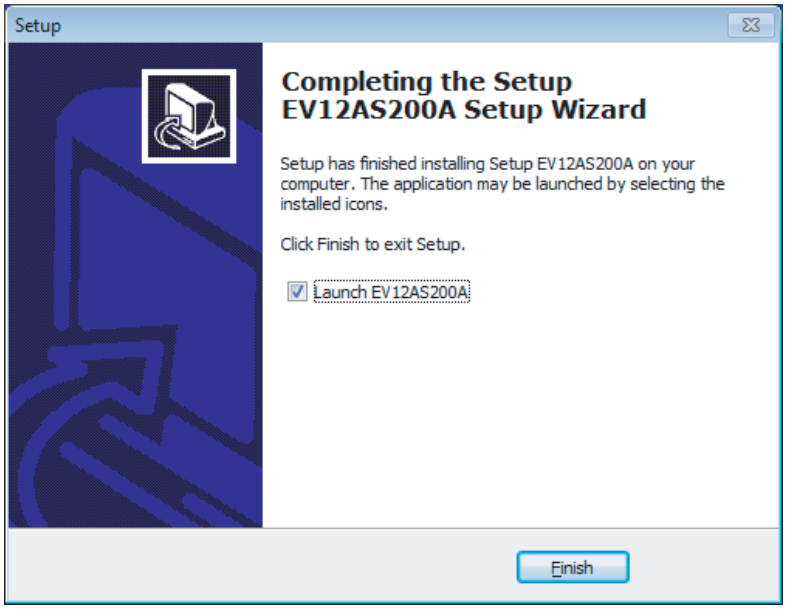


A black window may appear shortly. It's normal, and is part of installation process.

When all tasks are done, the following dialog appears.

If you wish to start application now, you should plug your device on any USB port of your workstation, and follow driver installation process. Otherwise, EV12AS200A application will claim no device is connected.

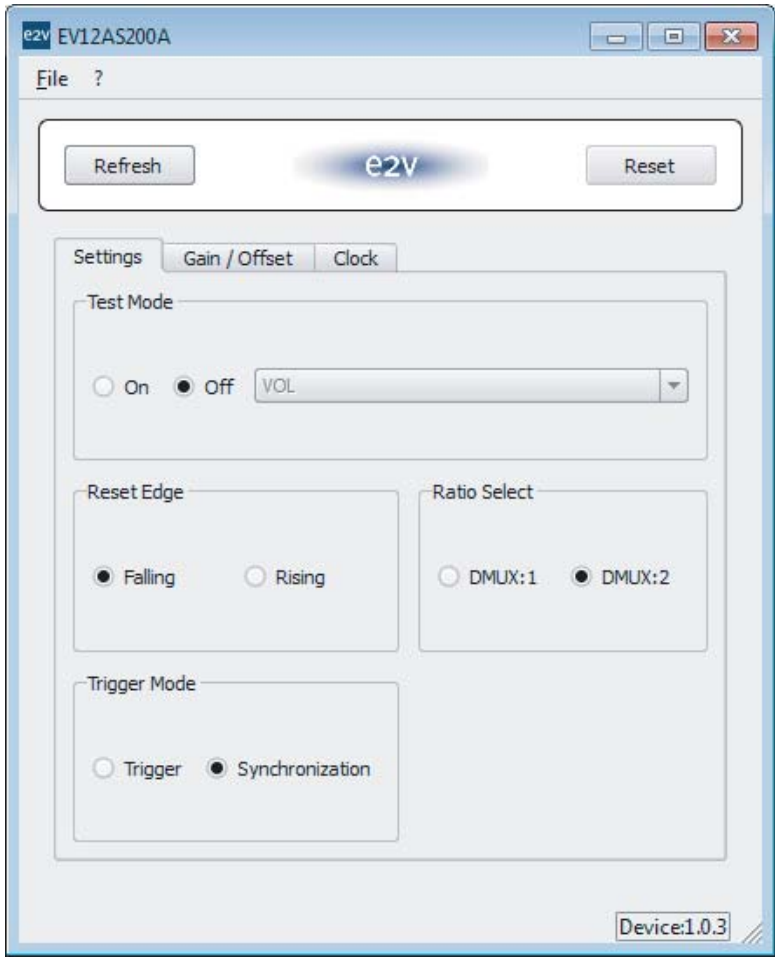
Figure 4-8. EV12AS200A Completing Setup Wizard Window



Setup is now completed successfully. After the installation,

You can launch the interface with the following file:
C:\Program Files\e2v\Setup_EV12AS200A_1.0.5.exe or you can click "icon" on desk top. The window shown in Figure 4-9 will be displayed.

Figure 4-9. EV12AS200A User Interface Window



4.3 Troubleshooting

1. Check that you own rights to write in the directory
2. Check for the available disk space
3. Check that at least one mini USB port is free and properly configured
4. Check that all supplies are properly powered on

Figure 4-10. EV12AS200A User Interface Hardware Implementation

1. Use an mini USB port to send data to the ADC.
2. Connect the crossed mini USB cable between your PC and your evaluation board.
3. Mode_n activated: JUMPER ON. (if no connected, use functionalities commands on board).

4.4 Operating Modes

The EV12AS200A software included with the evaluation board provides a graphical user interface to configure the ADC.

Push buttons, popup menus and capture windows allows easy:

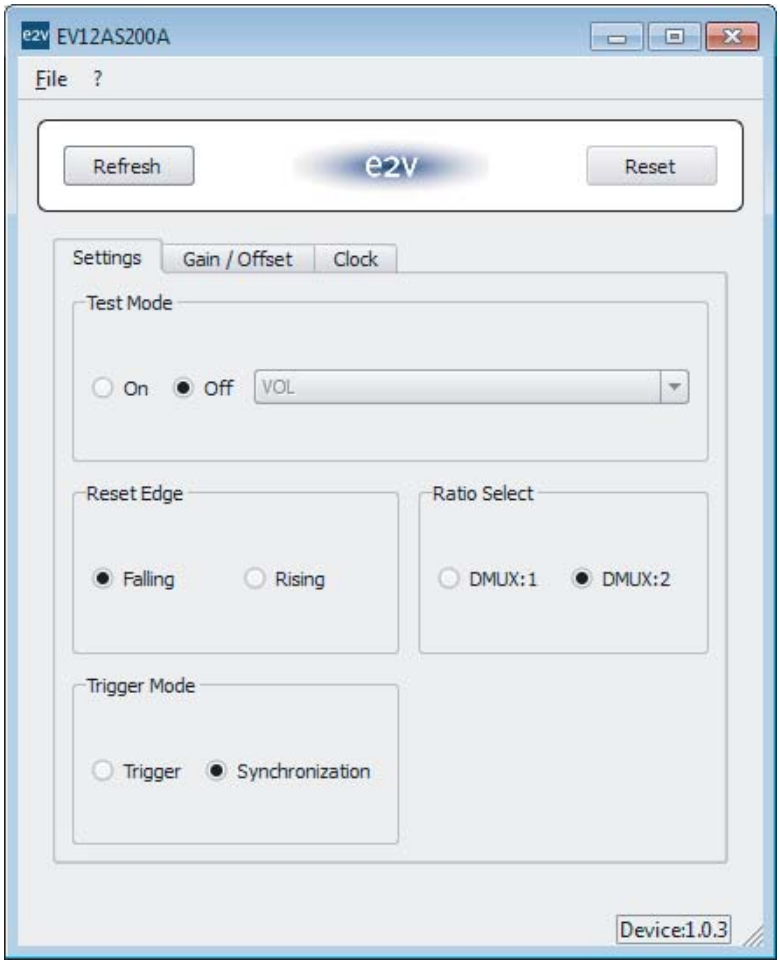
1. Settings
2. Gain / Offset
3. Clock

"Reset" button allows reconfiguring ADC to Default Mode.

"Reset" button allows checking ADC Mode.

4.4.1 Settings mode

Figure 4-11. Settings



In this window, six functions are available:

■ Ratio Select

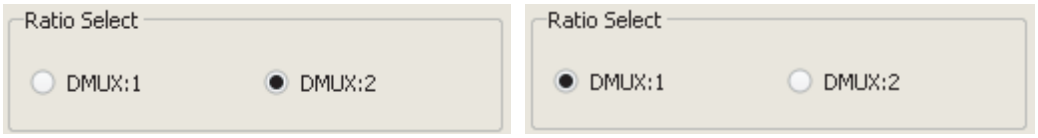
Two Demux Ratios can be selected. "Default value: DMUX1:2"

1:1 DMUX => Data only port A (Data0, Data1, Data2,…..)

1:2 DMUX => Data port A (Data0, Data2, Data4,….)

Data port B (Data1, Data3,….)

Figure 4-12. Ratio Select



■ Test mode

Default value: functionality => off

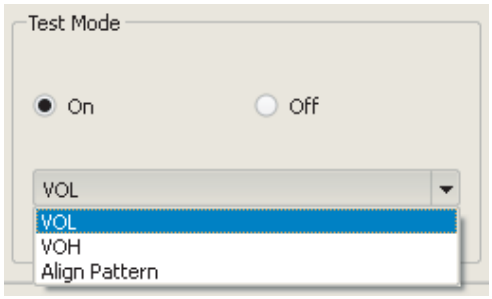
When "Test mode" is set to "On", three possibilities are available for data output:

All datas to VOL

All datas to VOH

Align pattern: Basic sequence of 16 cycles of output data rate.

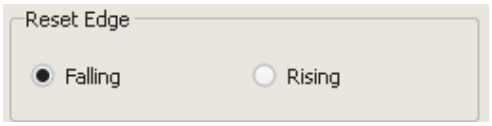
Figure 4-13. Test Mode



■ Reset Edge

This function allows changing the active edge of the SYNC signal. "Default value: functionality => Falling"

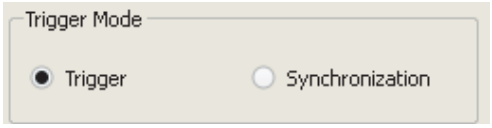
Figure 4-14. Reset Edge



■ Trigger Mode

This function allows to help synchronize multiple ADCs. "Default value: functionality => Synchronization"

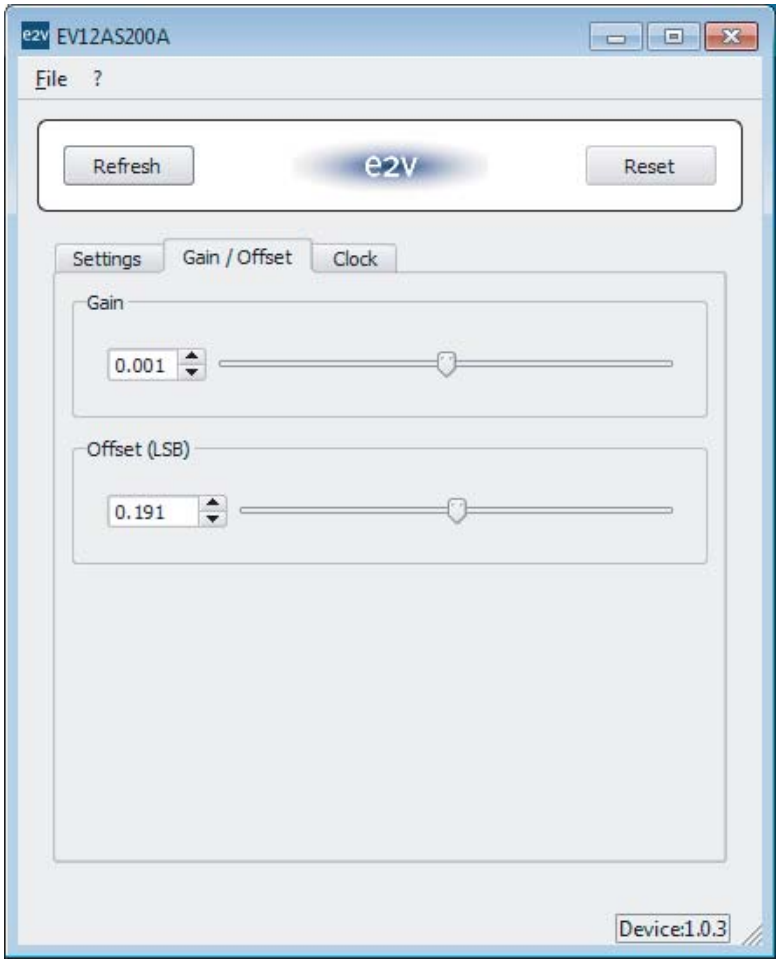
Figure 4-15. Trigger Mode



4.4.2 Gain / Offset

In this window, you can adjust the gain and offset.

Figure 4-16. Gain / Offset



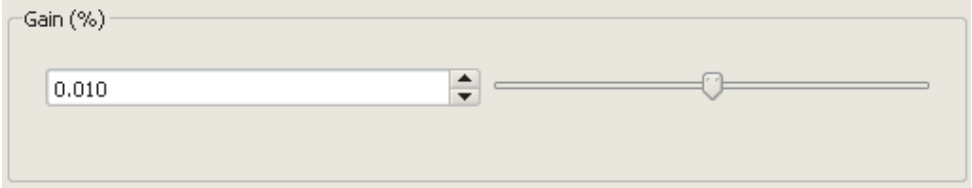
■ **Gain**

This function allows adjusting ADC Gain so that it can always be tuned to 1.0

The ADC Gain can be tuned by ±10% by tuning the voltage applied on GA by ± 0.5V around 2*Vcc3/3.

The step is 0.8LSB

Figure 4-17. Gain Initial



■ **Offset**

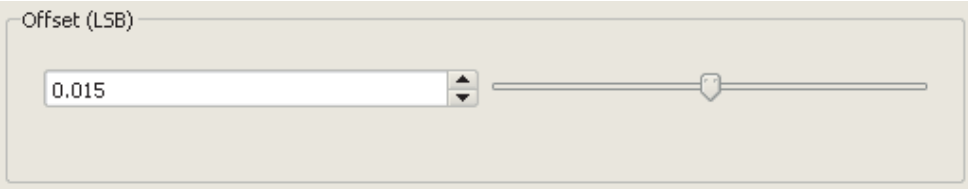
This function allows adjusting ADC Offset so that it can always be tuned to mid-code 2048.

The ADC Offset can be tuned by ±195 LSB (± 23.8 mV) by tuning the voltage applied on OA by ± 0.5V around 2*Vcc3/3.

2*Vcc3/3+0.5V gives the most negative offset variation and 2*Vcc3/3-0.5V gives the most positive offset variation

The ADC offset can be tuned by ±195LSB by step of 0.38LSB.

Figure 4-18. Offset Initial



4.4.3 Clock

In this window, you can adjust sampling delay and swing.

■ Sampling delay adjust

Sampling delay adjust (SDA pin) allows to tune the sampling ADC aperture delay (TA) around its nominal value.

This feature is particularly interesting for interleaving ADCs to increase sampling rate

Default value: functionality: Off

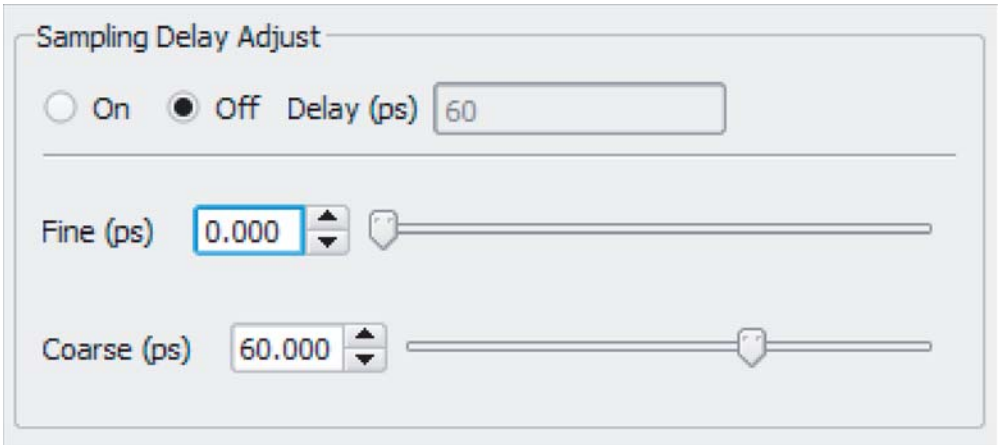
Figure 4-19. SDA Enable

Total SDA delay is given by SDA coarse value in addition to SDA fine value.

(case 6 -> delay)

SDA coarse register [1:0] allows a variation step of 0, 30 ps, 60 ps or 90 ps.

SDA fine register [9:0] allows fine step of 30 fs between a ranges from 0 to 30 ps



Section 5
Application Information

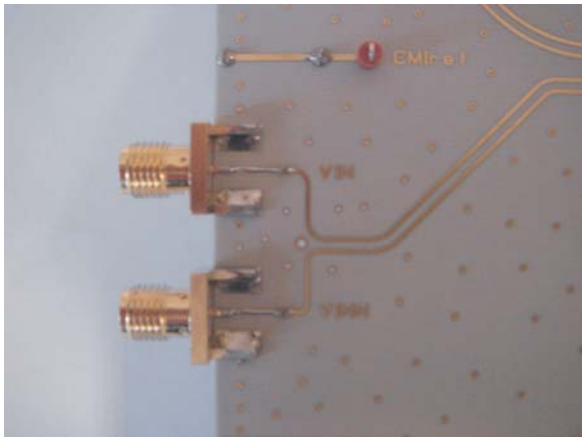
5.1 Analogue Input

The analogue input (VIN, VINN) are entered in differential AC coupled mode as described in Figure 4-1.

It is recommended to use a differential source to drive the analogue inputs of this ADC (external balun or differential amplifier). Please refer to Section Test Bench Description for more information.

In order to optimize the performance of the ADC, it is also recommended to use a band pass filter on the analogue input path.

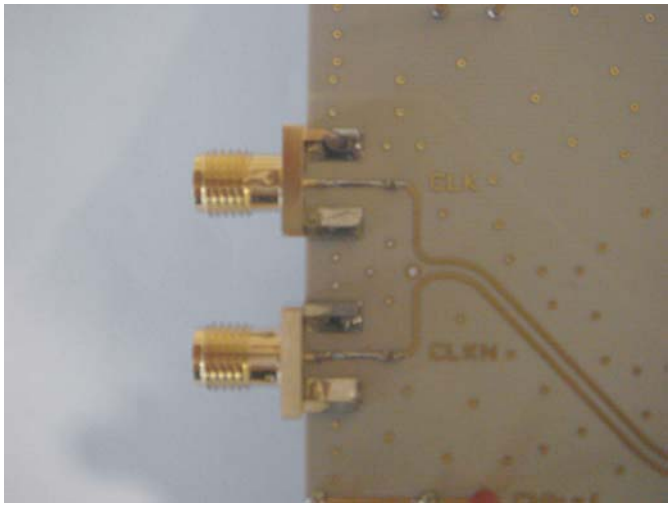
Figure 5-1. Differential Analogue Inputs Implementation



5.2 Clock Input

It is recommended to use a differential source to drive the clock input. The clock is AC coupled via 10 nF capacitors. Please refer to Section Test Bench Description for more information.

Figure 5-2. Clock Input Implementation

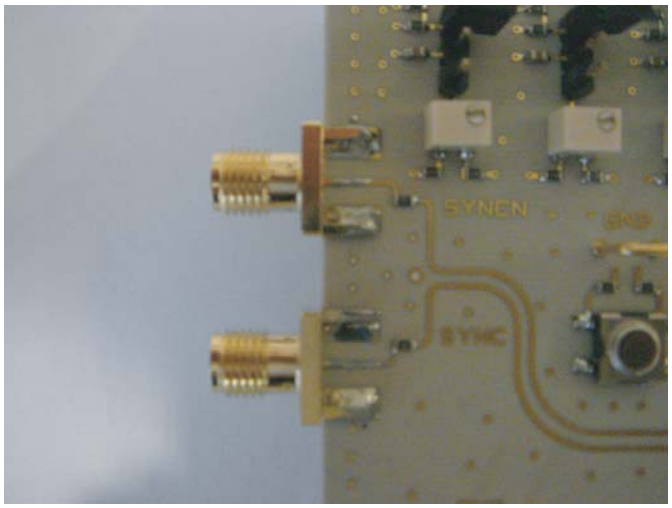


The jitter performance on the clock is crucial to obtain optimum performance from the ADC. We thus recommend to use a very low phase noise clock and to filter the clock signal if a fixed frequency is used.

5.3 SYNC input

An external LVDS reset (SYNC, SYNCN) is available in case it is necessary to reset the ADC during operation (it is not mandatory to perform an external reset on the ADC for proper operation of the ADC as a power up reset is already implemented). This reset is LVDS compatible. It is active low. It is asynchronous but is re-latched internally to the sampling clock.

Figure 5-3. RESETN Input Implementation

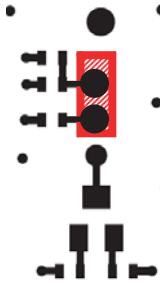


5.4 GA, OA, SDA and SDAEN pin Commands

These signals are connected by default via their respective jumper.

Mode_n deactivated: JUMPER OFF for switched SPI towards board.

Figure 5-4. Functionality Deactivated



Jumper: Functionality deactivated -> No variation of voltage range (set to default middle value 2 x V_{CC3}/3 = 2.2V)

Figure 5-5. Functionality Activated

Jumper: Functionality activated -> Variation of voltage range with tuneable resistor between (2 x V_{CC3}/3 - 0.5V = 1.7V) and (2 x V_{CC3}/3 + 0.5V = 2.7V)

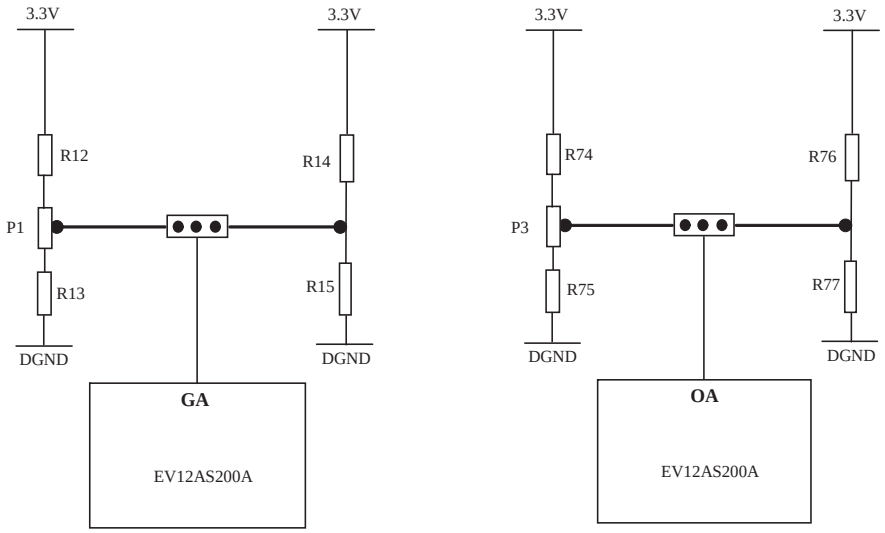
Figure 5-6. Functionality Floating

No Jumper: floating voltage = 2.16V

5.4.1 GA and OA Commands

These signals are connected by default via their respective jumper to the command middle value (ie. 2 x V_{CC3}/3 = 2.2V). When the jumper is removed, it is possible to tune the OA and GA commands between (2 x V_{CC3}/3 - 0.5V) to (2 x V_{CC3}/3 + 0.5V).

Figure 5-7. GA and OA Commands Implementation



With:

R12 = R74 = 287Ω

R14 = R76 = 649Ω

P1 = P3 = 1K

R13 = R75 = 1.05 kΩ

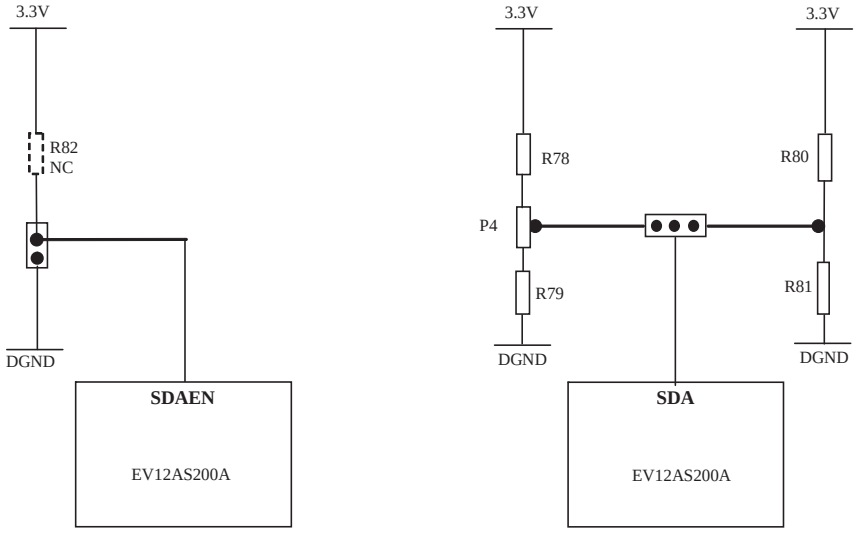
R15 = R77 = 1.33 kΩ

5.4.2 SDAEN and SDA Commands

SDAEN signal allows activating the SDA command when its jumper is OUT or connected. When the SDA function is activated via SDAEN, then it is possible to tune the sampling delay of the ADC by tuning the SDA command between (2 x V_{CC3}/3 - 0.5V) and (2 x V_{CC3}/3 + 0.5V) by 40 ps around the nominal Aperture delay of the ADC.

1133BX–BDC–12/14

Figure 5-8. SDAEN and SDA Commands Implementation



With:

R82 = 10 kΩ (NC: can be connected to provide a true High level to SDAEN)

R78 = 287Ω

R80 = 649Ω

P4 = 1K

R79 = 1.05 kΩ

R81 = 1.33 kΩ

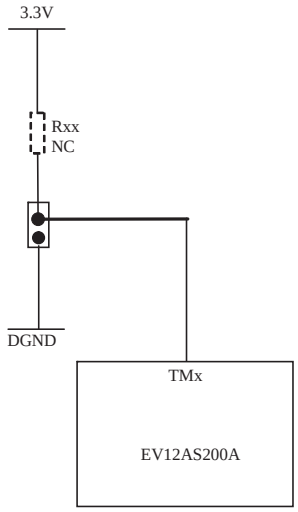
Figure 5-9. SDAEN Command Jumper Settings

SDAEN activated: JUMPER ON SDAEN inactivated: JUMPER OUT

5.5 RS, TM, and MODE_n Commands

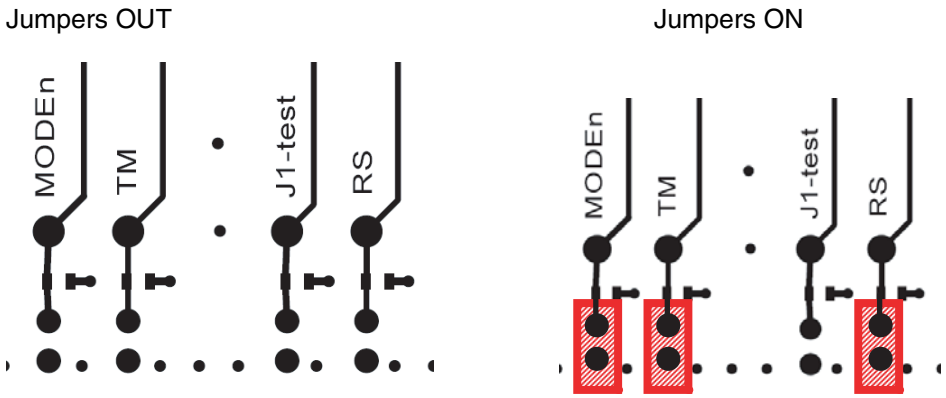
The RS, TM, and MODE_n functions are implemented on board with a jumper which can be ON or OUT (default setting is when the Jumpers are OUT). A 10 kΩ resistor can be connected in case a pull up is necessary to force a high level on these signals. This resistor is not connected.

Figure 5-10. RSx, TMx, and MODE_n, Commands Implementation



■ The default setting for RS, TM and MODE_n is when their respective jumper is OUT.

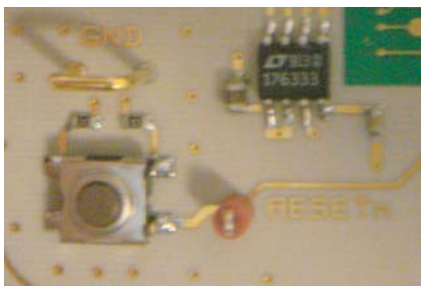
Figure 5-11. RS, TM and MODE_n Command Jumper Settings



5.6 RESETn

The RESETn signal allows reconfiguring ADC to Default Mode.

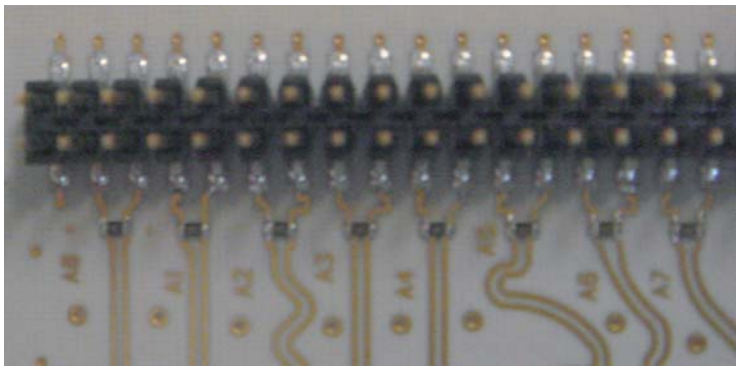
Figure 5-12. RESETn Command



5.7 Output Data

The digital outputs are compatible with LVDS standard. They are on-board 100 differentially terminated.

Figure 5-13. Differential Digital Outputs Implementation



Double row 2.54 mm pitch connectors are used for the digital output data. The lower row is connected to the signal while the upper row is connected to Ground.

The connectors are vertical connectors.

Figure 5-14. Differential Digital Outputs 2.54 mm Pitch Connector (X = A, B)

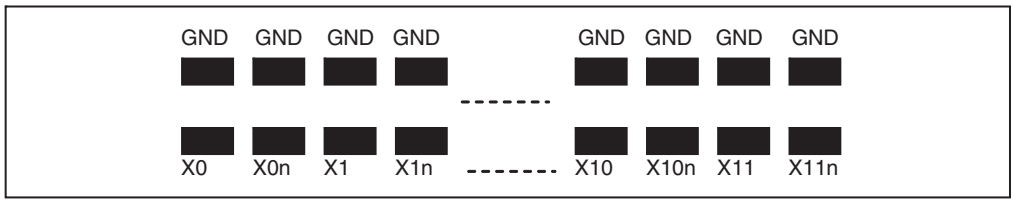


Figure 5-15. Differential Digital Outputs 2.54 mm Pitch Connector (Port A)

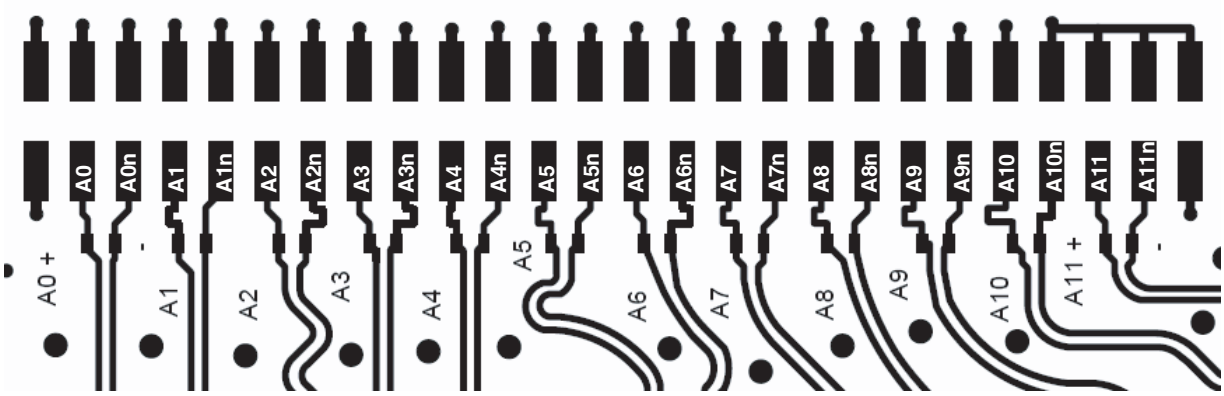


Figure 5-16. Differential Digital Outputs 2.54 mm Pitch Connector (Port B)

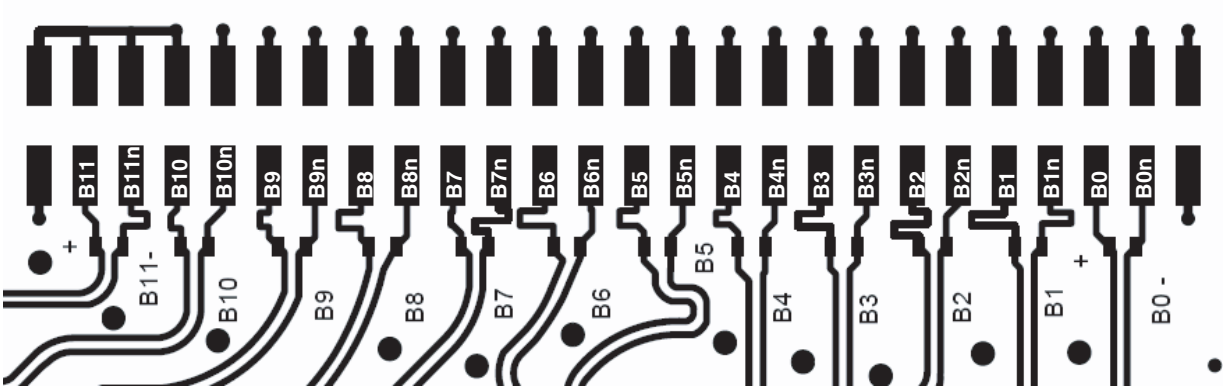


Figure 5-17. Differential Digital Outputs 2.54 mm Pitch Connector (DR, DRN Signal)

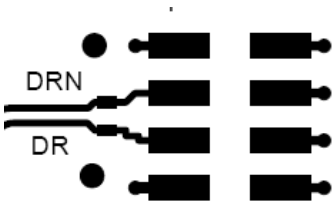


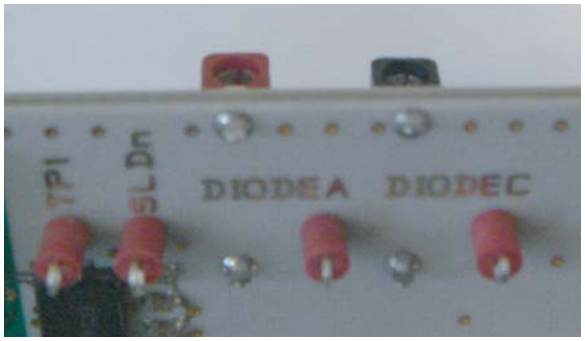
Figure 5-18. Differential Digital Outputs 2.54 mm Pitch Connector (PCBa, PCBan, PCBb, PCBbn Signal)

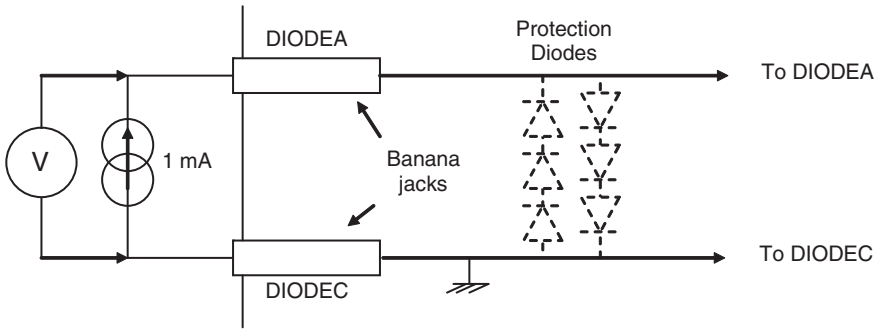
5.8 Diode for Junction Temperature Monitoring

Two 2 mm banana jacks are provided for the die junction temperature monitoring of the ADC.

One banana jack is labeled DIODEA and should be applied a current of up to 1 mA (via a multimeter used in current source mode) and the second one is connected to DIODEC.

Figure 5-19. Die Temperature Monitoring Test Setup

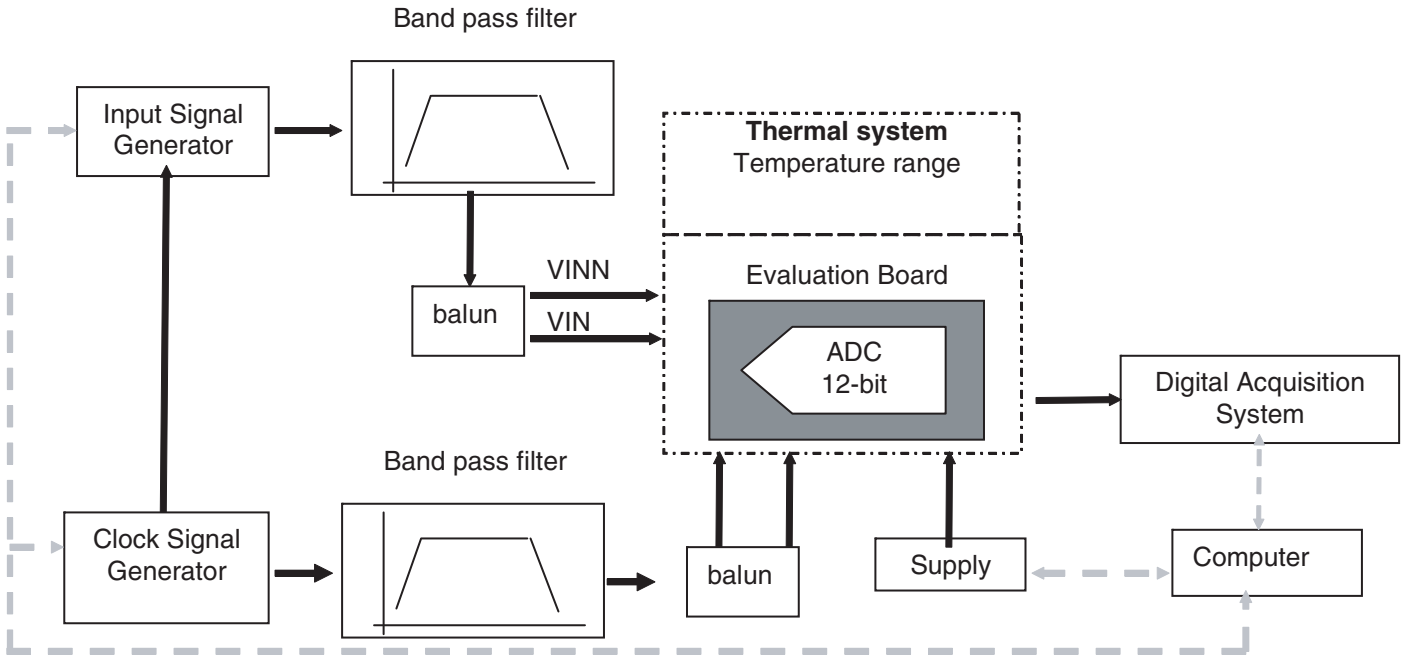




Note: The protection diodes are NC.

5.9 Test Bench Description

Figure 5-20. Test Bench Description



■ Equipment

Input Signal Generator: Agilent E4426B or E4424B

Clock Signal Generator: Agilent E4426B or MARCONI 2042

Power Supply: Agilent 6629A

Logic Analyzer: HP16500C or TLA7012

Balun: MACOM-H9 (2MHz => 2GHz)

Band pass filter: LORCH (500MHz => 1GHz) & LORCH (1GHz => 2GHz)

Section 6
Ordering Information

Table 6-1. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
EVX12AS200AZPY-EB	fpBGA196 RoHS	Ambient	Prototype	Evaluation board for EV12AS200A family

Please refer to the datasheet 1122 for product ordering information.

6.1 Revision History

This table provides revision history for this document.

Table 6-2. Revision History

Rev. No	Date	Substantive Change(s)
1133BX	10/2014	CA adjust removed in accordance to latest datasheet
1133AX	02/2014	Initial revision

Section 7

Appendix

7.1 EV12AS200AZPY-EB Electrical Schematics

Figure 7-1. Power Supplies Bypassing

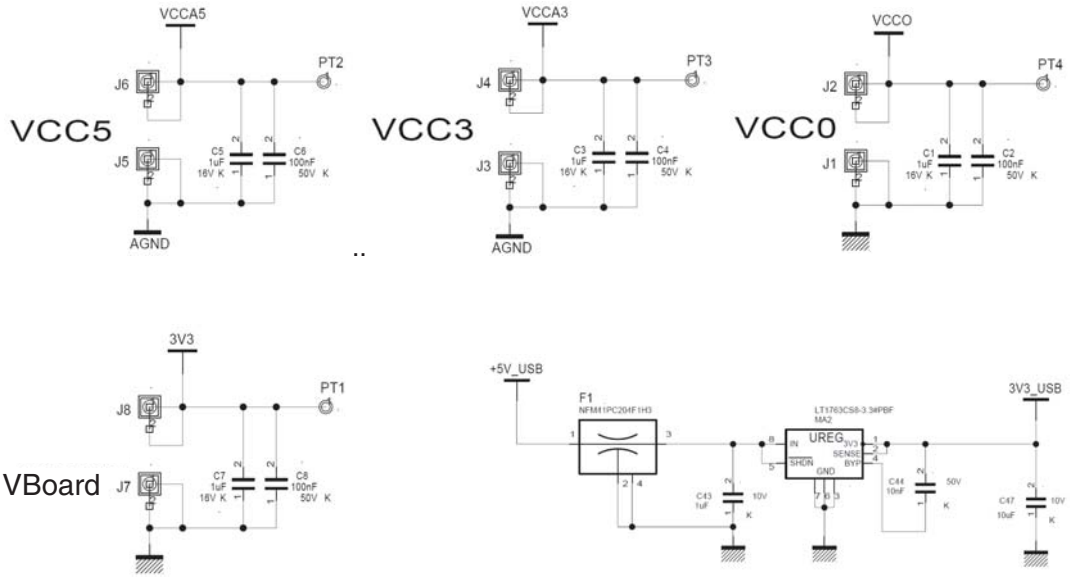


Figure 7-2. Power Supplies Decoupling

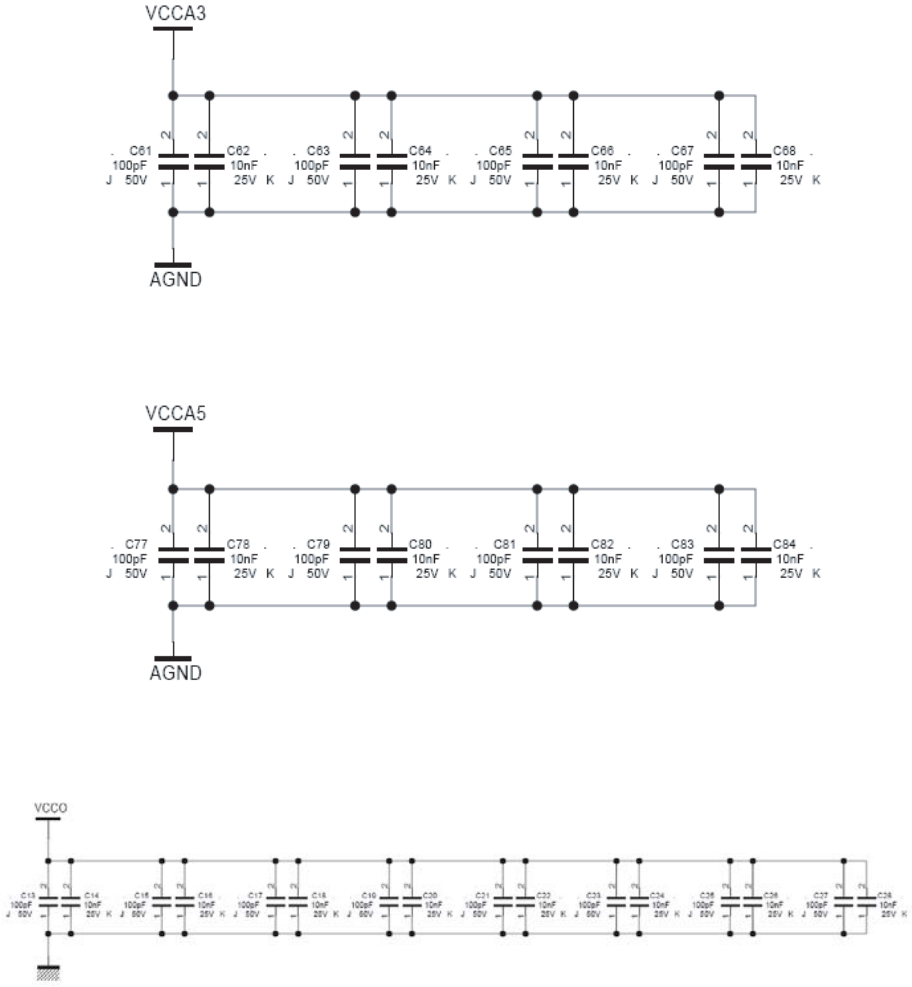
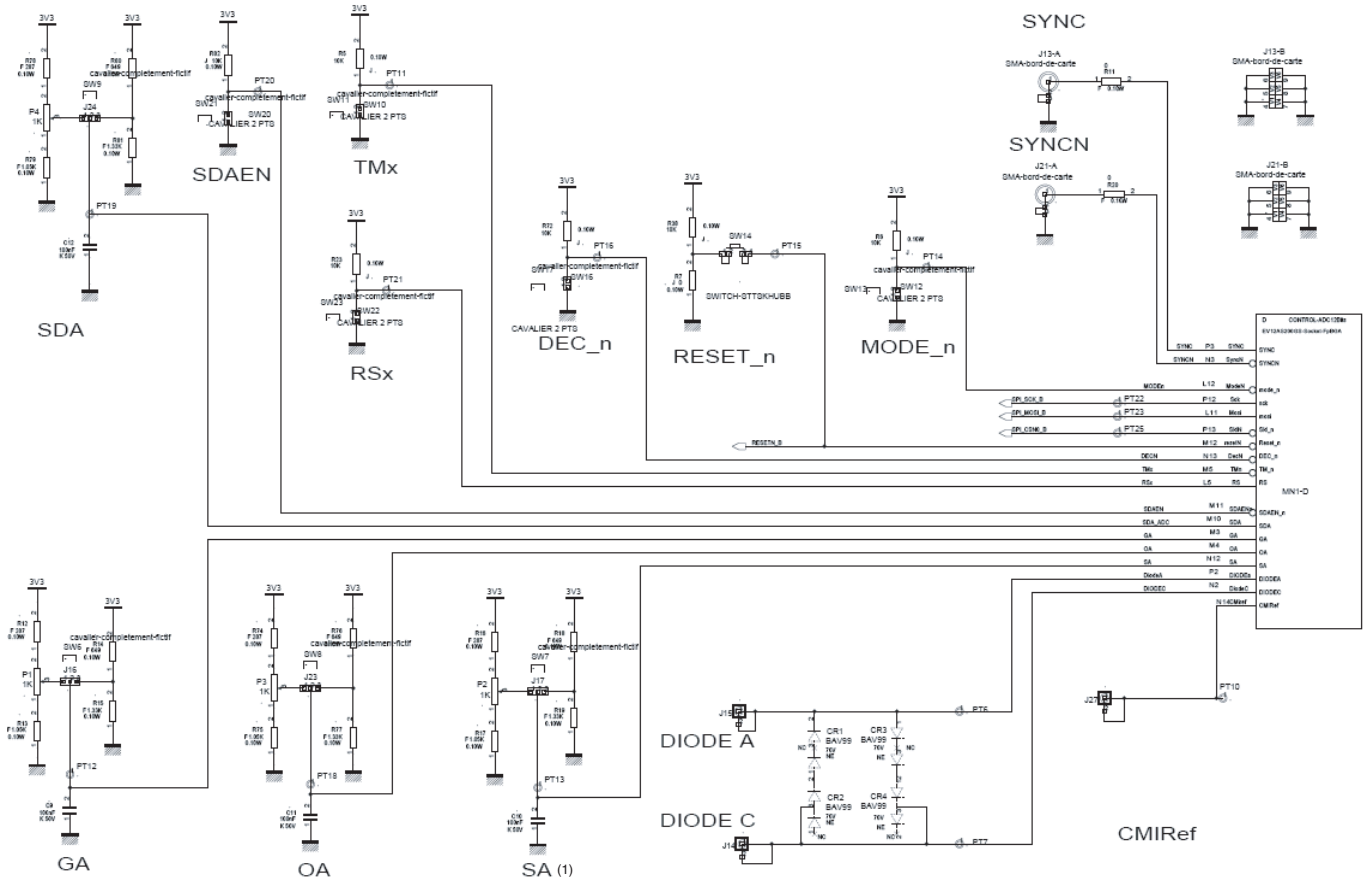


Figure 7-3. Electrical Schematics (Control)



(1) For e2v purpose only.

Figure 7-4. Electrical Schematics (Analogue and clock input)

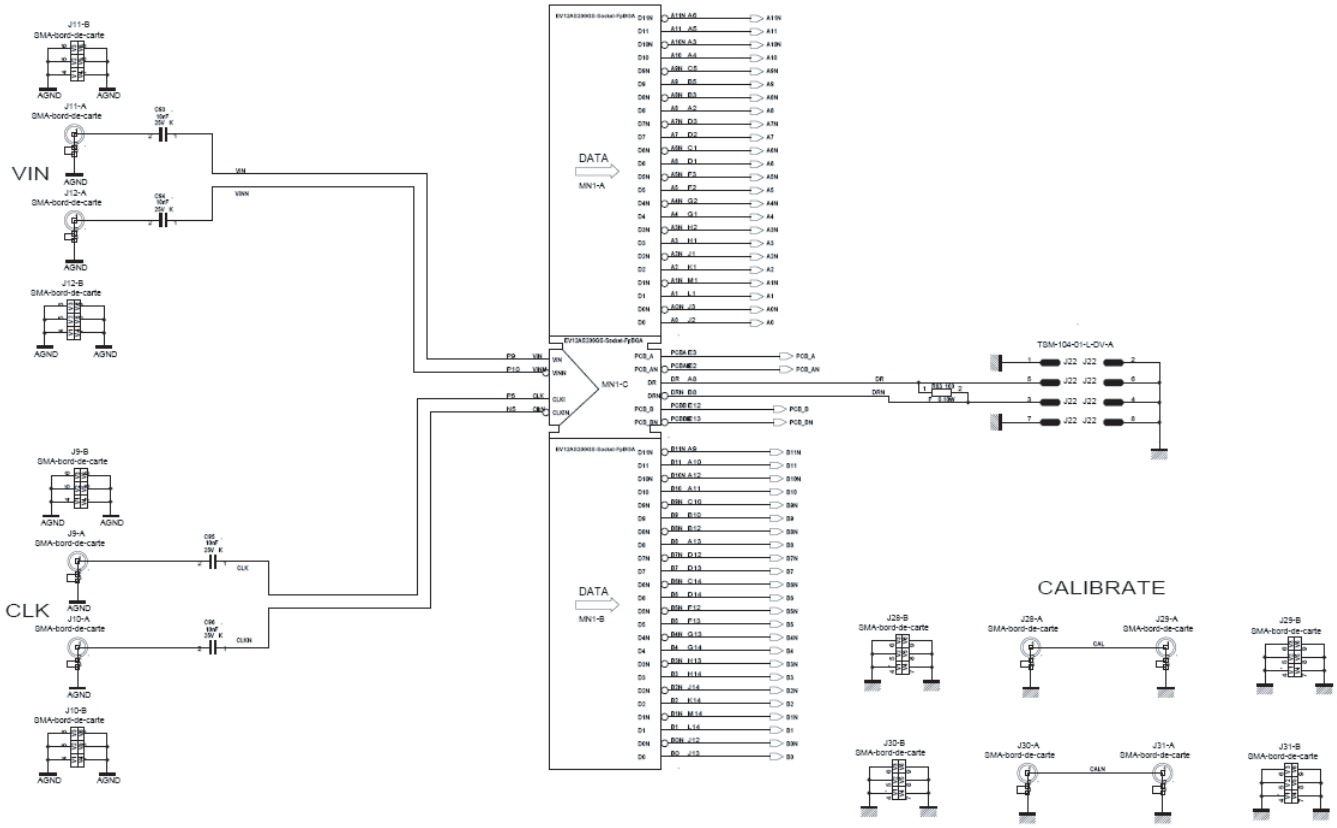


Figure 7-5. Electrical Schematics (SPI)

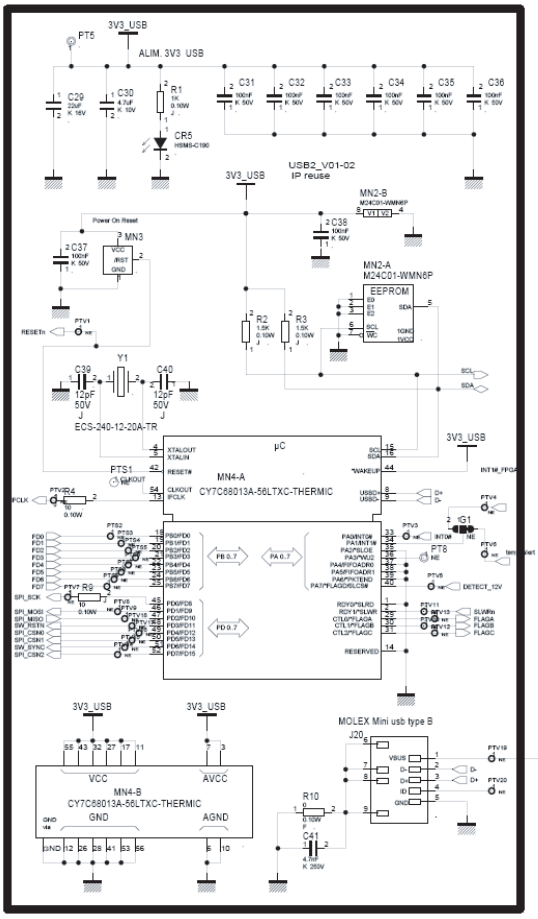


Figure 7-6. Electrical Schematics (SPI Level Translator)

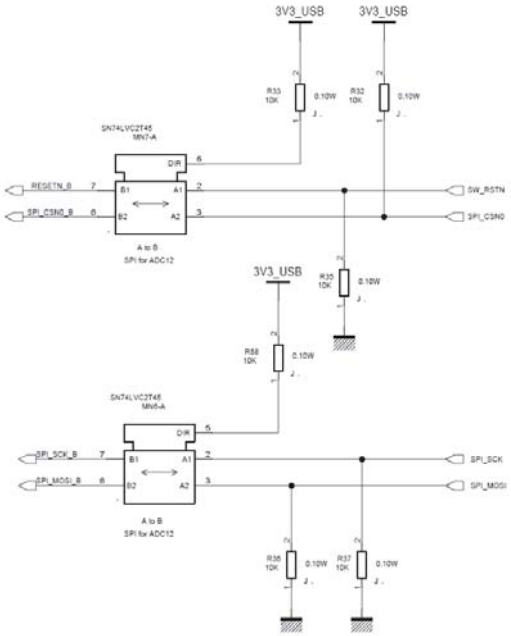
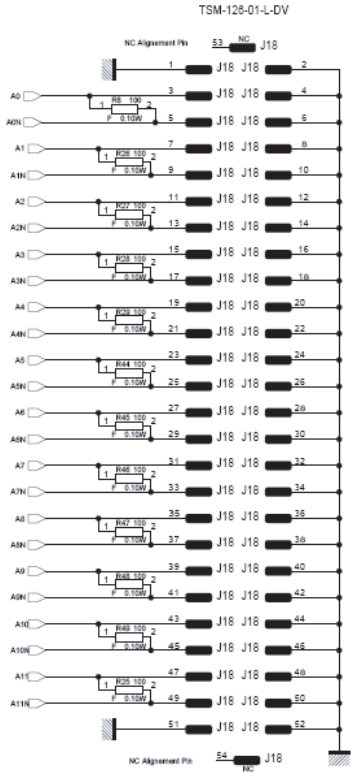
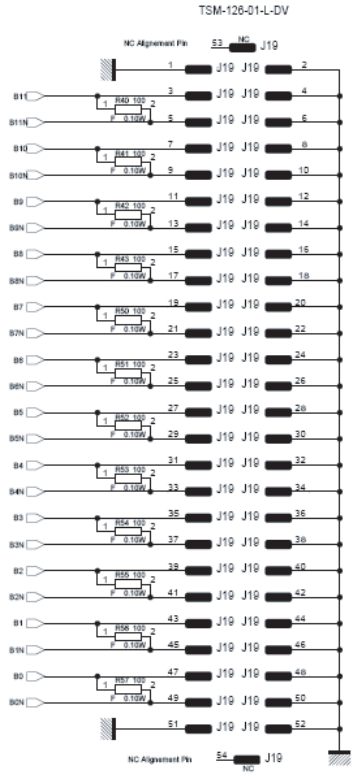


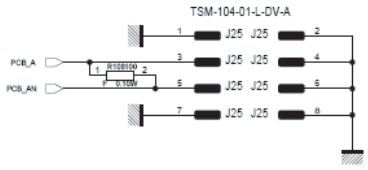
Figure 7-7. Electrical Schematics (Output Connectors Ports A and B)



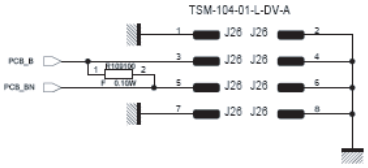
PORT A



PORT B



PARITY CHECK BIT A



PARITY CHECK BIT B

7.2 EV12AS200AZPY-EB Board Layers

Figure 7-8. Top Layer

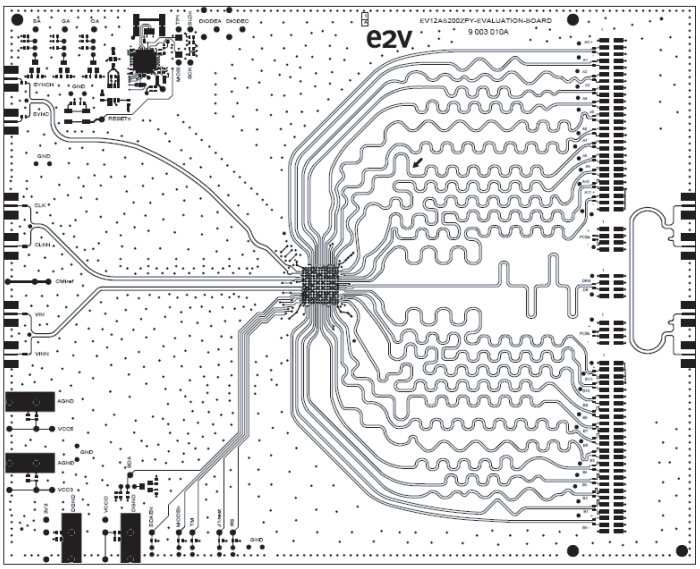
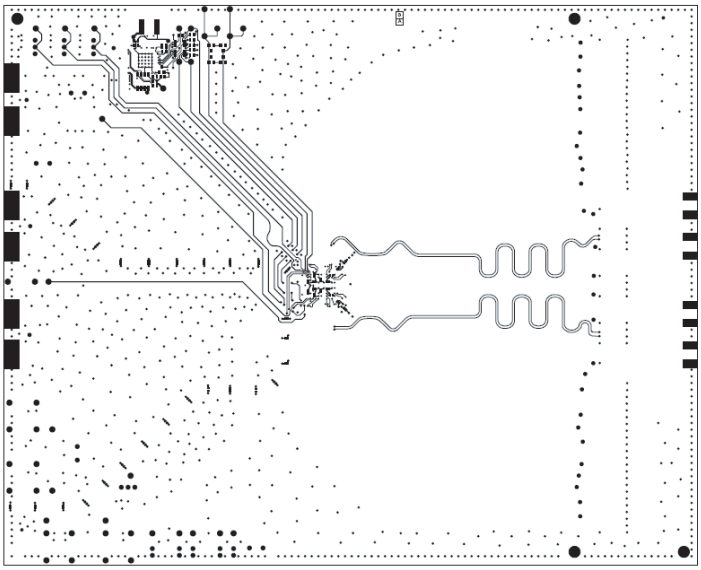


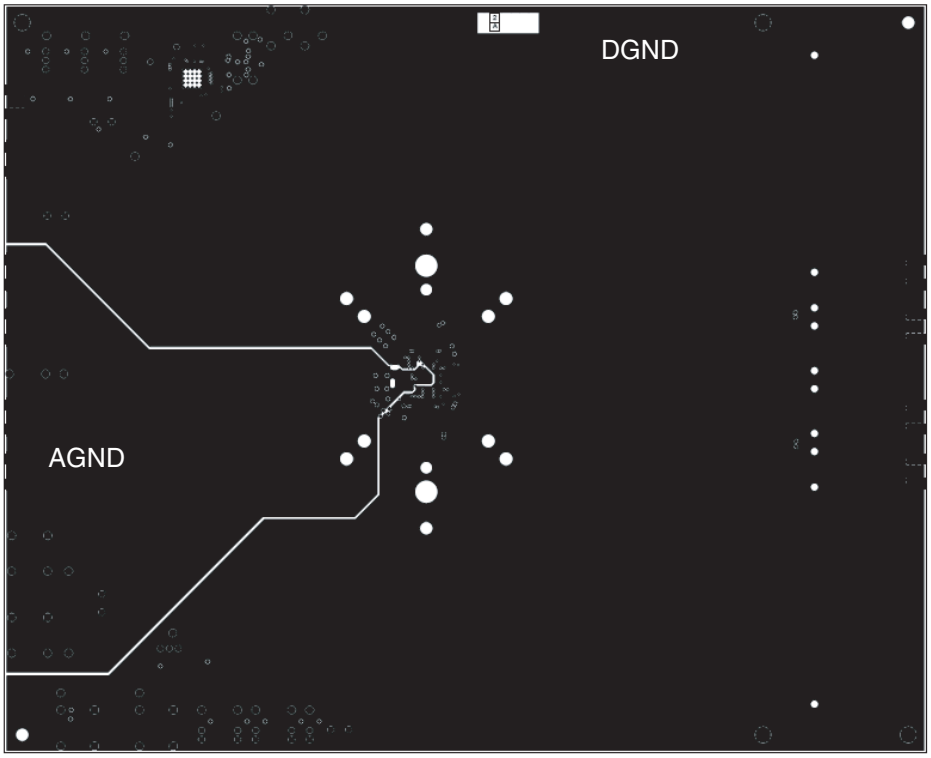
Figure 7-9. Bottom Layer



1133BX–BDC–12/14

Figure 7-10. AGND, DGND (Separate Planes) LAYER 2 & 5

Layer 2



Layer 5

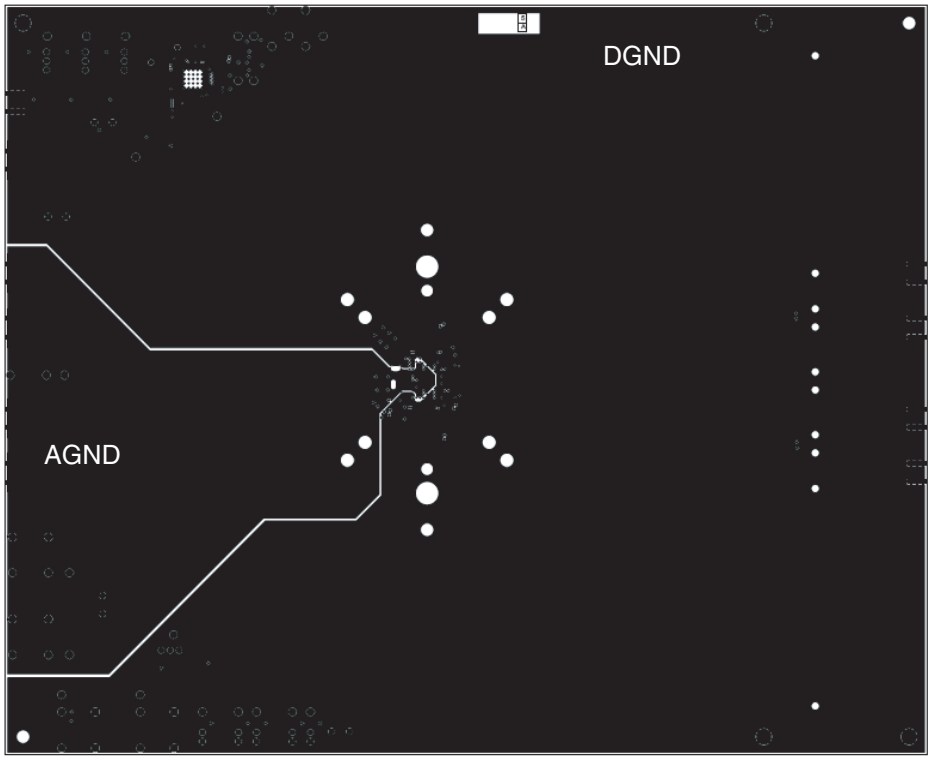
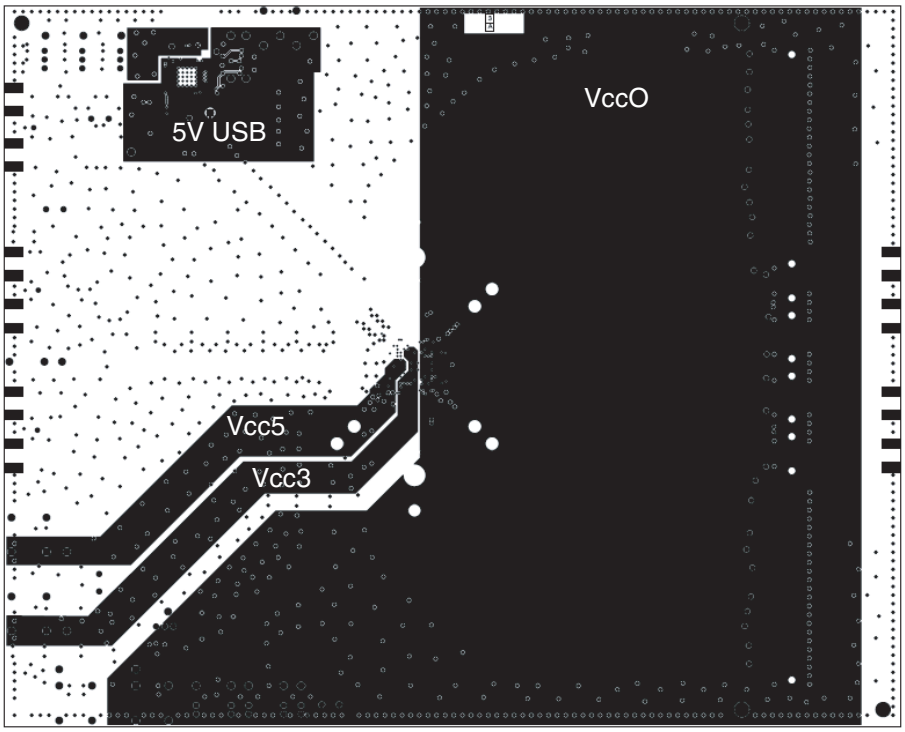


Figure 7-11. Power Supplies LAYER 3 & 4

Layer 3: V_{CC5}, V_{CC3}, V_{CCO} and 5V USB



Layer 4: 3V3

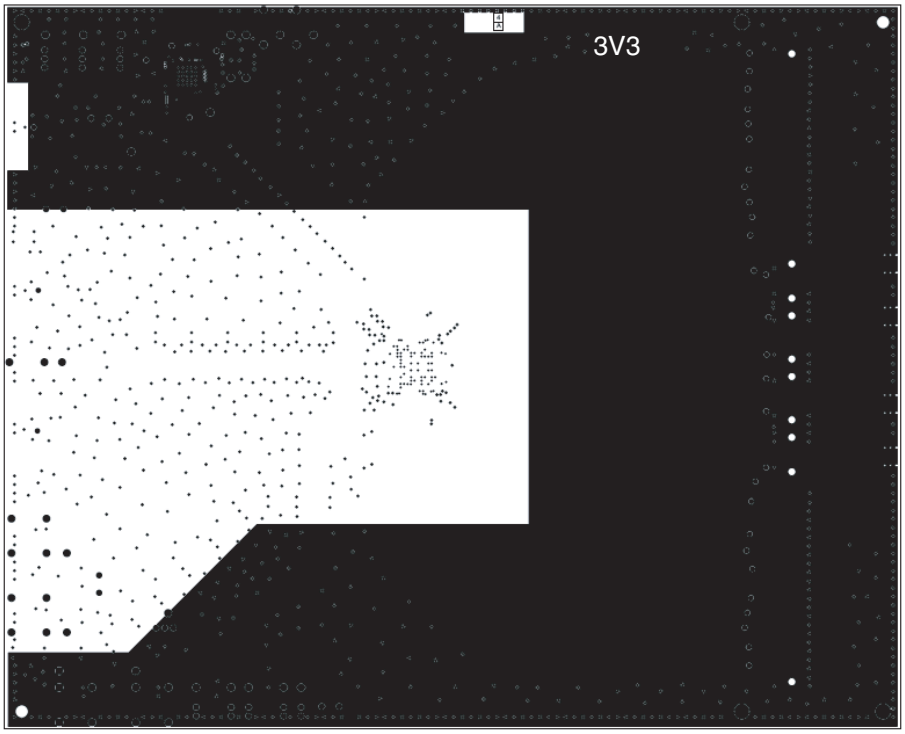


Figure 7-12. Equipped Board (Top)

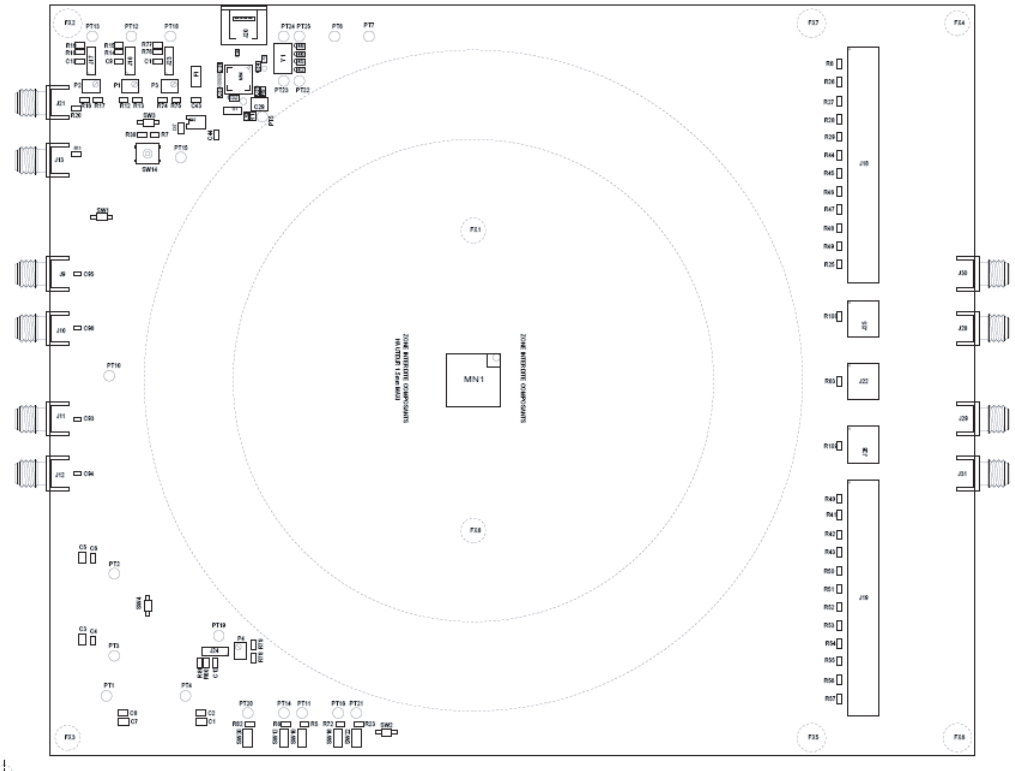
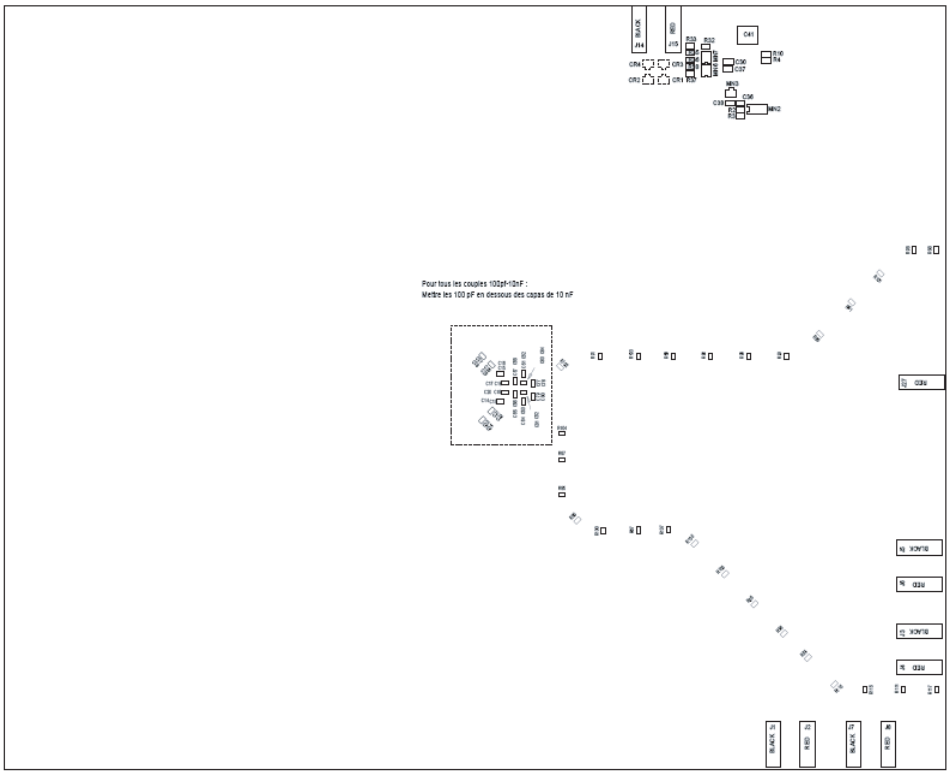


Figure 7-13. Equipped Board (Bottom)



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