EV8AQ160CTPY
CALIBRATION Methodology for Interleaving QUAD 8-bit 1.25 Gsps ADC

Application Note

This Application Note gives you recommendations to perform Calibration for interleaving the QUAD 8-bit 1.25 Gsps ADC (EV8AQ160CTPY).

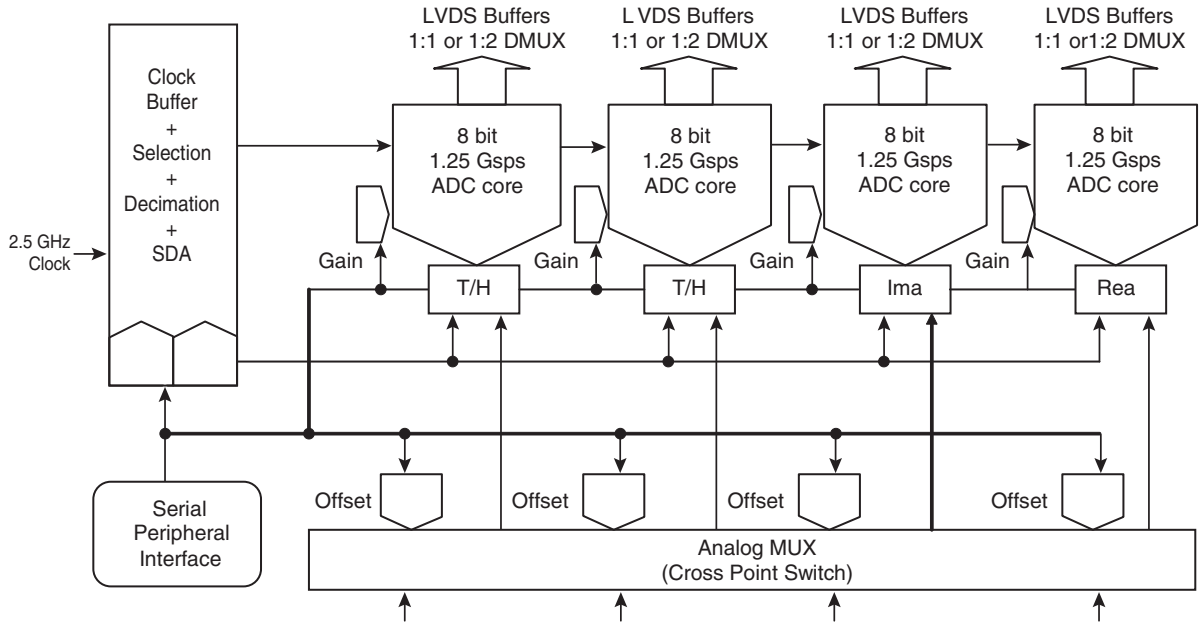
1. QUAD 8-bit EV8AQ160CTPY

The Quad ADC EV8AQ160CTPY is made up of four 8-bit ADC cores which can be considered independently (4-channel mode) or grouped by 2 cores (2-channel mode with the ADCs interleaved two by two or 1-channel mode where all four ADCs are all interleaved).

Quad ADC EV8AQ160CTPY with 8-bit resolution

- 1.25 Gsps Sampling Rate in 4-channel mode
- 2.5 Gsps Sampling Rate in 2-channel mode
- 5 Gsps Sampling Rate in 1-channel mode

Figure 1-1. Simplified Block Diagram



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The Time-interleaved ADC System can exhibit imperfect artifacts (distortion) in the frequency domain if the individual ADC core characteristics are not well matched. Offset, Gain and Phase (delay) are of primary concern.

This Application Note attempts to give you a methodology to calculate the correct Offset, Gain and Phase value of each ADC to perform an interleaving ADC without FFT degradation.

1.1 Interleaving Calibration

Interleaving the 4 internal ADCs of EV8AQ160CTPY needs to be calibrated with Offset, Gain and Phase matching.

→ Each ADC must have as close as possible the same Offset, Gain and Phase.

The following examples show you the difference between an incorrect calibration and a correct interleaving calibration.

Figure 1-2 shows in time domain the result of 1Channel configuration of EV8AQ160CTPY without Calibration of 600 MHz sine wave sampling at 2.5 GHz.

Figure 1-2. Time Domain of 1Channel Configuration of EV8AQ160CTPY without Calibration

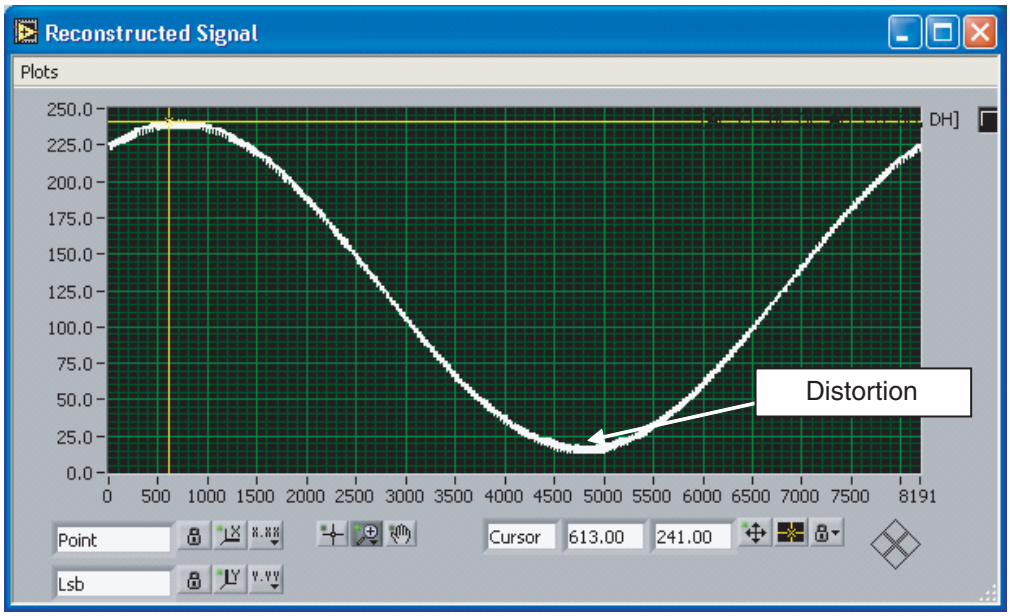


Figure 1-3 shows in time domain the result of 1Channel configuration of EV8AQ160CTPY with Calibration of 600 MHz sine wave sampling at 2.5 GHz.

Figure 1-3. Time Domain of 1Channel Configuration of EV8AQ160CTPY with Calibration

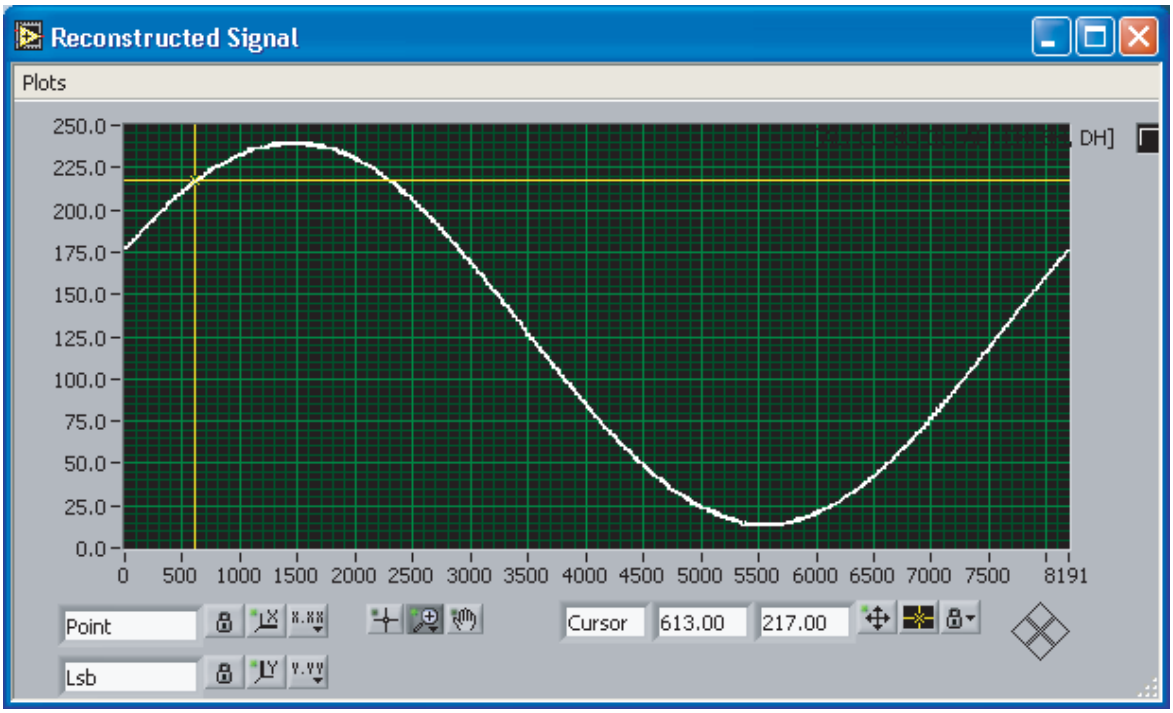


Figure 1-4 shows the FFT resulting with 1Chanel configuration of EV8AQ160CTPY without Calibration of 600 MHz sine wave sampling at 2.5 GHz.

Figure 1-4. FFT of 1Channel Configuration of EV8AQ160CTPY without Calibration

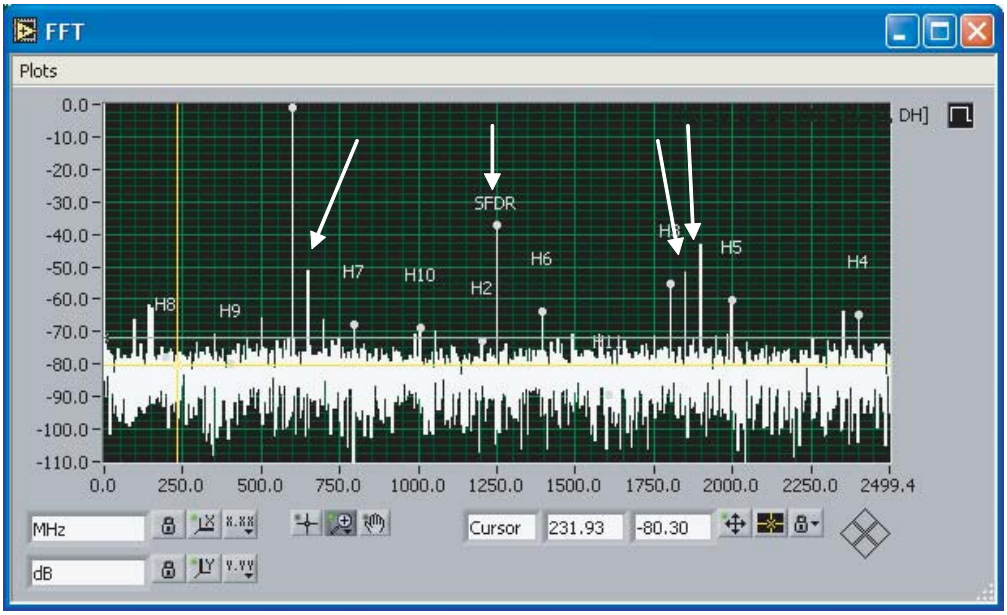
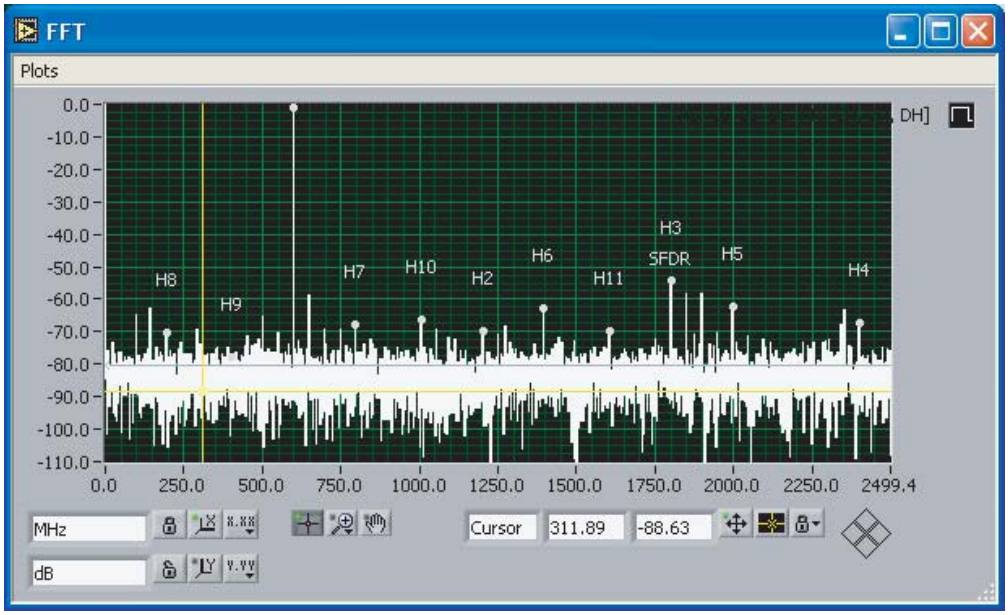


Figure 1-5 shows the FFT resulting of 1Chanel configuration of EV8AQ160CTPY with Calibration of 600 MHz sine wave sampling at 2.5 GHz.

Figure 1-5. FFT of 1Channel Configuration of EV8AQ160CTPY with Calibration



FFT parameter without calibration

[AL, CL, BL, DL, AH, CH, BH, DH]

	Frequency (Mhz)	dB
H0	0.000000	3.04
H1	600.585937	-1.12
H2	1201.171875	-69.48
H3	1801.757812	-55.22
H4	2402.343750	-65.29
H5	1997.070312	-61.13
H6	1396.484375	-63.16
H7	795.898437	-68.92
H8	195.312500	-77.90
H9	405.273437	-90.16
H10	1005.859375	-68.92

THD (dBc)	-51.94
THD (dBFS)	-53.06
SINAD (dBc)	34.42
SINAD (dBFS)	35.54
SFDR Frequency (Hz)	1.250000G
SFDR (dBc)	-36.29
SFDR (dBFS)	-37.42
SNR (dBc)	34.50
SNR (dBFS)	35.62
ENOB	5.42
ENOB_FS	5.61
SFSR (dBc)	-1.12

FFT parameter with calibration

[AL, CL, BL, DL, AH, CH, BH, DH]

	Frequency (Mhz)	dB
H0	0.000000	2.97
H1	600.585937	-1.07
H2	1201.171875	-69.79
H3	1801.757812	-54.15
H4	2402.343750	-67.48
H5	1997.070312	-62.16
H6	1396.484375	-62.89
H7	795.898437	-67.89
H8	195.312500	-70.37
H9	405.273437	-77.71
H10	1005.859375	-66.08

THD (dBc)	-51.24
THD (dBFS)	-52.31
SINAD (dBc)	42.96
SINAD (dBFS)	44.03
SFDR Frequency (Hz)	1.801758G
SFDR (dBc)	-53.08
SFDR (dBFS)	-54.15
SNR (dBc)	43.66
SNR (dBFS)	44.73
ENOB	6.84
ENOB_FS	7.02
SFSR (dBc)	-1.07

2. Offset Gain Phase Adjustment

The Offset, Gain Phase of each ADC are controlled through the Digital Interface (SPI).

The digital interface is a standard SPI (1.8V CMOS) with:

Four **DACs for the gain controls** are addressed thru the SPI:

Four **DACs for the offset controls** are addressed thru the SPI:

- Offset DACs act close to the cross point switch
- Gain DACs act on the biasing of the reference ladders of each ADC core

These DACs have a resolution of 8-bit and will allow the control via the SPI of the offset and gain.

- Gain adjustment on 256 steps, ±10% range
- Offset adjustment on 256 steps, ±40 mV range

Four **DACs for fine phase control** are addressed through the SPI, they have an 8-bit resolution

- Phase adjustment on 256 steps, ±15ps (1 step is about 120 fs)

The e2v evaluation board contains Graphical User Interface (GUI), which allows device adjustment through the SPI interface. The SPI adjustments are accessed using the internal register within the Offset Gain Phase sheet of GUI.

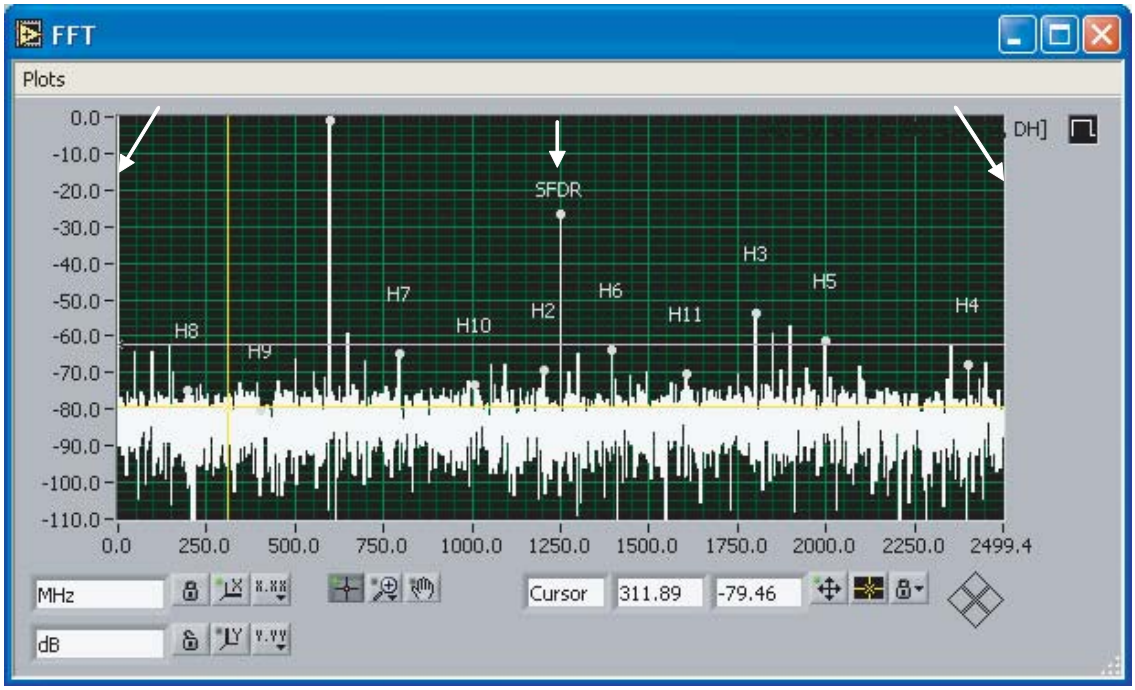
We can observe the influence of each parameter (Offset, Gain and Phase) on the FFT spectrum.

2.1 Offset Adjustment

The Figure 2-1 shows the FFT of QUAD 8bit sampling at 2.5 GHz a 600.59 MHz sinus wave. In this example the Offset mismatch between internal ADC has been intentionally increasing (by setting Channel A to –15.2) to illustrate the effect.

You could see the clock spur (Fc/2 = 1250 MHz) increasing.

Figure 2-1. Resulting FFT After Intentionally Offset Increasing



Conclusion:

The offset mismatching affects the spur Fc, Fc/2 and DC. Only clock spur Fc/2 affects the dynamic performance.

2.2 Gain Adjustment

Figure 2-2 shows the FFT of QUAD 8-bit sampling at 2.5 GHz a 600.51 MHz sinus wave. In this example the Gain mismatch between internal ADC has been intentionally increased (by setting Channel A to –5.941) to illustrate the effect.

You can observe the increases in the different fundamental image spurs.

F1 = Fc – Fin = 2500 MHz – 600.59 MHz = 1899.41 MHz

F2 = Fc/2 – Fin = 1250 MHz – 600.59 MHz = 649.41 MHz

F3 = Fc – F2 = 2500 MHz – 659.41 MHz = 1850.59 MHz

Note: Fc = external clock = 2.5 GHz and Fc/2 = Fs = internal clock of each ADC = 1.25 GHz.

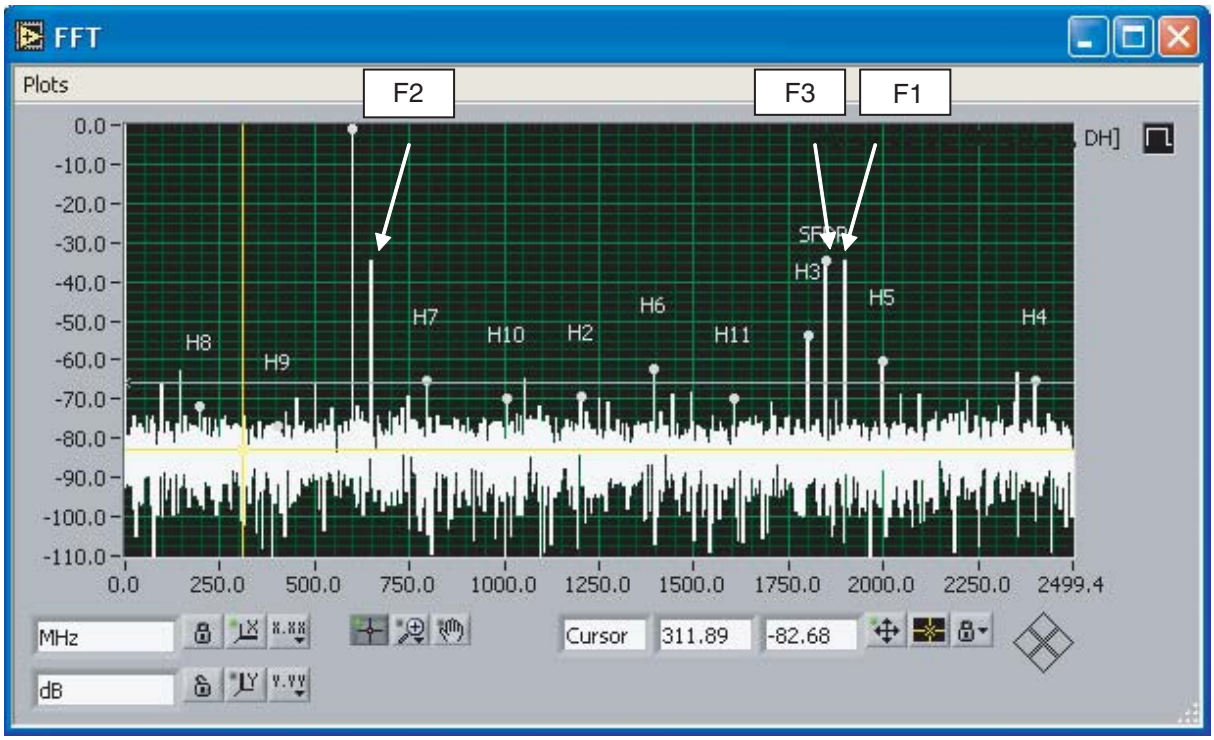
Note: In order to ensure that the analog input signal and the sampling clock are coherent signals (which implies that there is an integer number of analog signal cycles in the acquisition), the following calculation method needs to be respected:

$$\frac{Fin}{Fs} = \frac{M}{N}$$

With Fin = Analog signal frequency
Fs = Sampling frequency
M = Number of analog signal cycles, **M has to be odd**
N = Number of samples in acquisition

When this condition is fulfilled, the processing of the data sequence becomes easier since no windowing is required to deal with spectral splatter (no aliasing).

Figure 2-2. Resulting FFT After Intentionally Gain Increasing



Conclusion:

The Gain mismatching affects only the fundamental image spur.

2.3 Phase Adjustment

The Figure 2-3 shows the FFT of QUAD 8-bit sampling at 2.5 GHz a 600.59 MHz sinus wave. In this example the Phase mismatch between internal ADC has been intentionally increased (by setting Channel A to –5.118) to illustrate the effect.

You can observe the increases in the different fundamental image spurs

F1 = Fc – Fin = 2500 MHz – 600.59 MHz = 1899.41 MHz

F2 = Fc/2 – Fin = 1250 MHz – 600.59 MHz = 649.41 MHz

F3 = Fc – F2 = 2500 MHz – 659.41 MHz = 1850.59 MHz

Note: Fc = external clock = 2.5 GHz and Fc/2 = Fs = internal clock of each ADC = 1.25 GHz

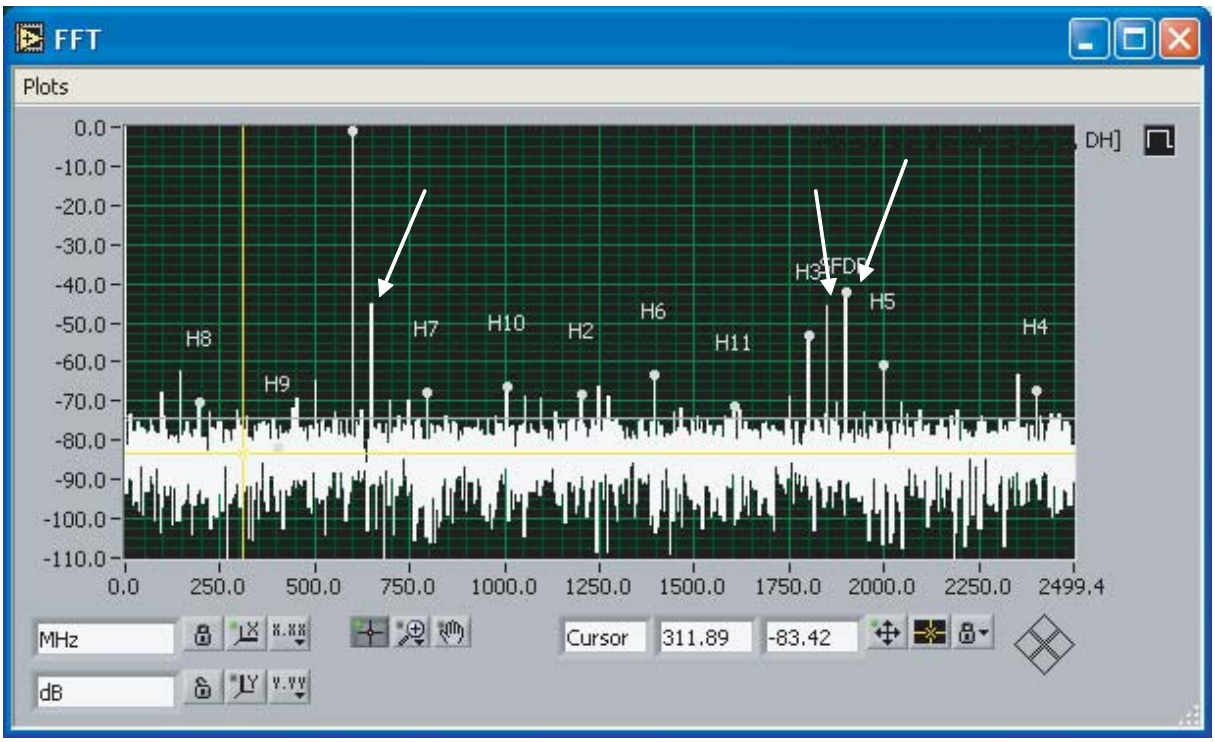
Note: In order to ensure that the analog input signal and the sampling clock are coherent signals (which implies that there is an integer number of analog signal cycles in the acquisition), the following calculation method has to be respected:

$$\frac{Fin}{Fs} = \frac{M}{N}$$

With Fin = Analog signal frequency
Fs = Sampling frequency
M = Number of analog signal cycles, **M has to be odd**
N = Number of samples in acquisition

When this condition is fulfilled, the processing of the data sequence becomes easier since no windowing is required to deal with spectral splatter (no aliasing).

Figure 2-3. Resulting FFT After Intentionally Phase Increasing



Conclusion:

The Phase mismatching affects only the fundamental image spur.

3. Calibration

This chapter shows the calibration methodology to calibrate Offset Gain Phase of each ADC.

To calibrate an Offset Gain and Phase, we need to have a sinus wave reference signal.

The frequency of this signal is very important for Phase calibration, it must be equal to the maximum frequency used in your system (in this example we use a sinus wave at 600 MHz).

The calibration must be done in this order: Offset first, then Gain and finally Phase.

In Demux 1:2 configuration, for channel A you must take data come from AL and AH.

3.1 Offset Calibration

The goal of Offset calibration is to have the same offset for the 4 internal ADC (Channel A B C D).

→ Offset equal to middle range = 127.5

Apply an analog sinus wave (Ex: 600.59 MHz sinus wave) and capture the output data for each ADC (QUAD in configuration 1 channel but calculation done separately on Channel A, B, C and D).

Calculate the average code of each ADC (Channel A B C D), this average must be equal to 127.5.

Change the offset (via SPI) to set all ADC with average =127.5 (± 0.1LSB).

Figure 3-1. Reconstructed Signal without Offset Calibration

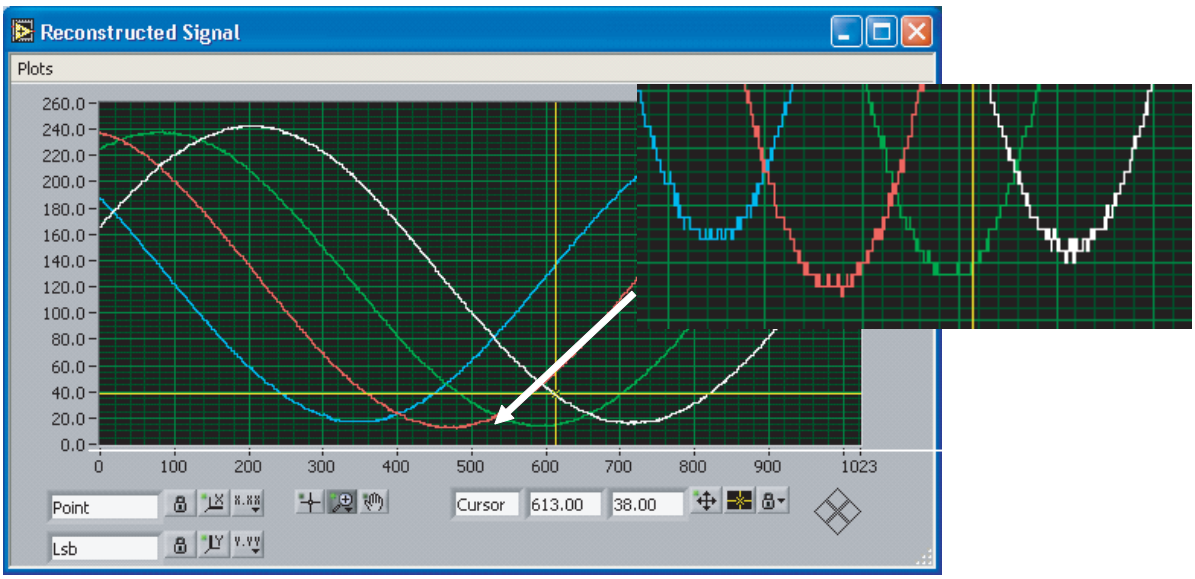
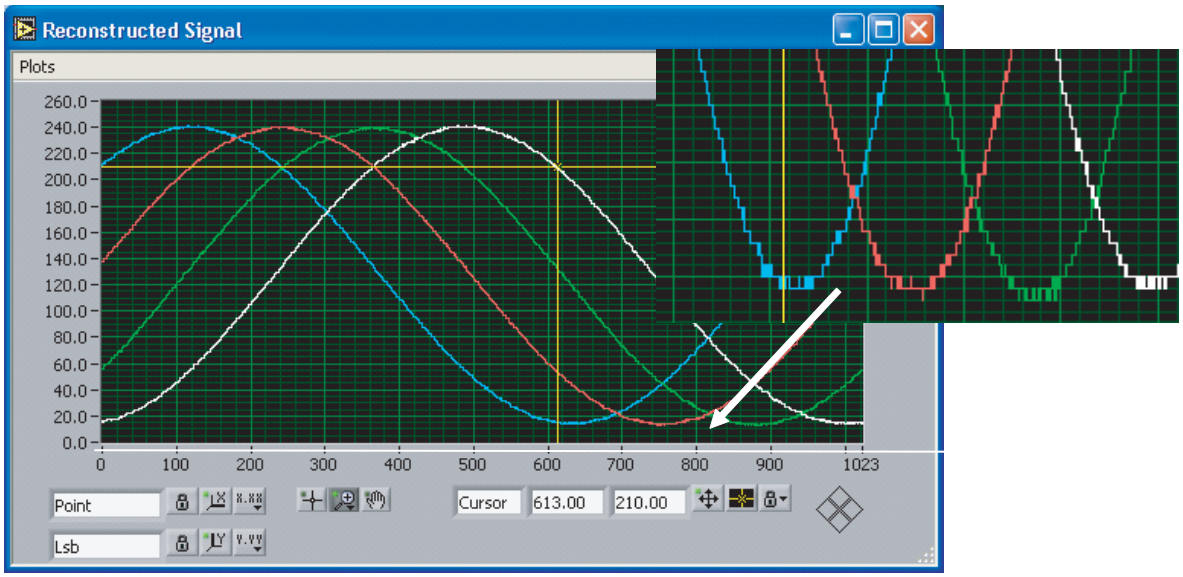


Figure 3-2. Reconstructed Signal with Offset Calibration



3.2 Gain Calibration

The goal of the Gain calibration is to have the same Gain for the 4 internal ADC (Channel A B C D).

→ Channel A is taken as a reference and the Gain of B C D is adjusted to be equal to Channel A.

Apply an analog sinus wave (Ex: 600.59 MHz sinus wave) and capture the output data for each ADC (QUAD in configuration 1 channel but calculation FFT done separately on Channel A, B, C and D).

For each ADC (separately not interleaved) calculate the FFT spectrum and calculate the power of fundamental spur (module).

Take the A channel as a reference and change the Gain (via SPI) to set the channel B, C, D ADC with the same power of the fundamental channel A (± 0.05dB).

Figure 3-3. Resulting FFT without Gain Calibration

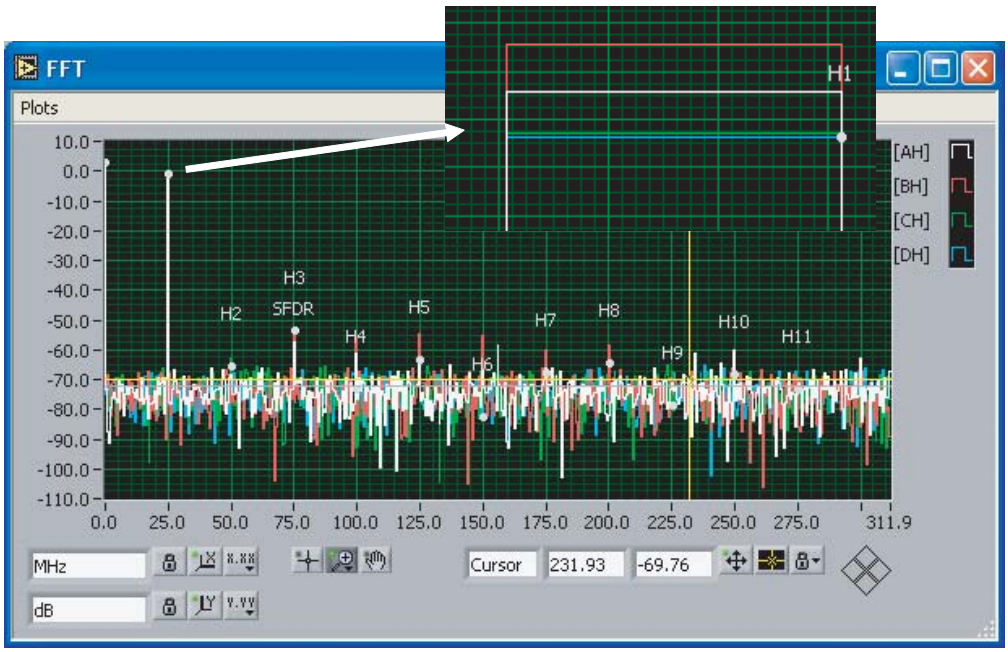
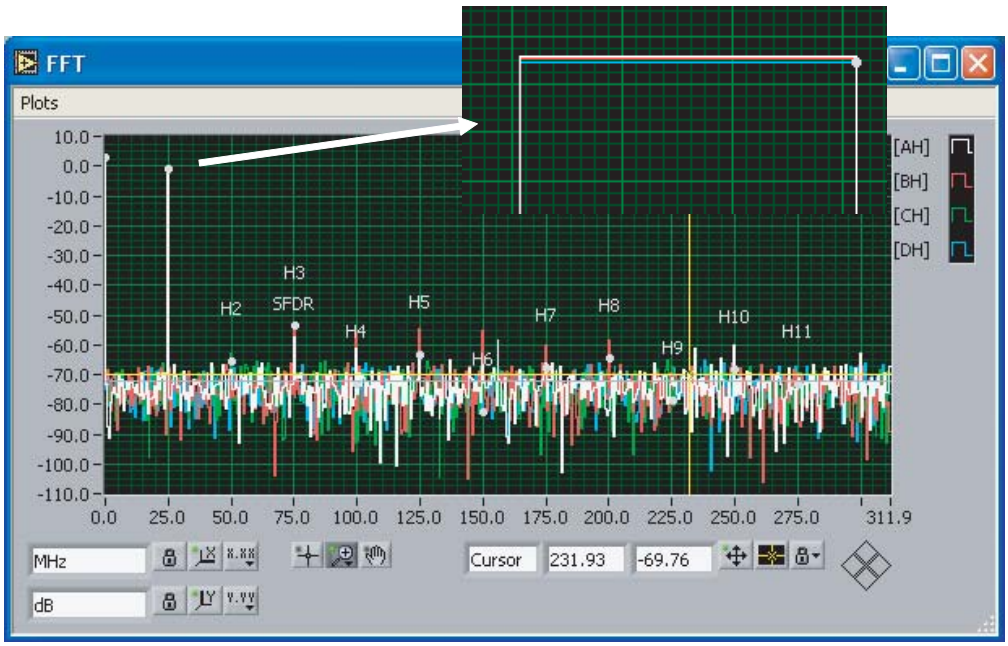


Figure 3-4. Resulting FFT with Gain Calibration



3.3 Phase calibration

The goal of Phase calibration is to have the same difference in Phase between the 4 internal ADC (Channel A B C D).

→ Channel A is taken as reference and the difference in Phase between channel A-C, C-D, C-D and D-A must be the same.

Apply an analog sinus wave (Ex: 600.59 MHz sinus wave) and capture the output data for each ADC (ADC separately channel A B C D).

For each ADC (separately not interleaving) calculate the FFT spectrum (Phase) and calculate the Phase of fundamental spur.

The difference of Phase between Channel A and C is equal to $\Pi/2 + \Delta\Phi 1$

The difference of Phase between Channel C and B is equal to $\Pi/2 + \Delta\Phi 2$

The difference of Phase between Channel B and D is equal to $\Pi/2 + \Delta\Phi 3$

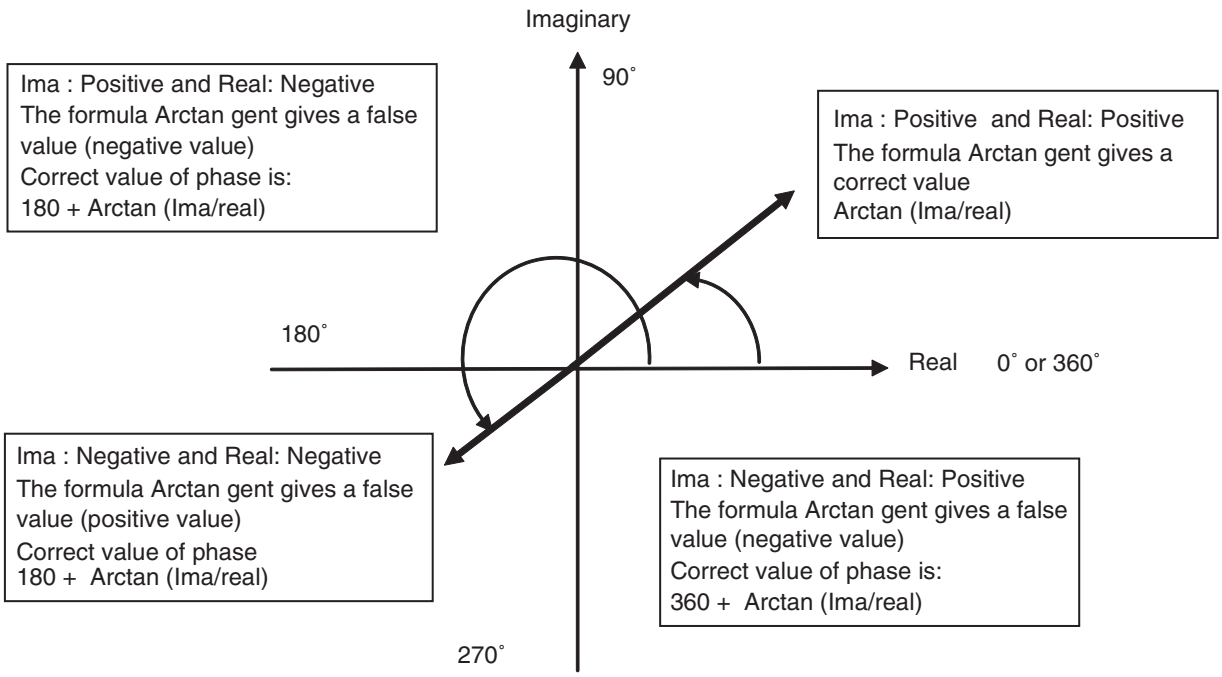
The difference of Phase between Channel D and A is equal to $-\Pi/2 + \Delta\Phi 4$

Note: $\Delta\Phi$ is the error of phase for each channel.

Calculating of the phase is not an easy calculation. Phase in degree is given by this formula:

$180/\Pi \times$ Arctan (Imaginary Number / Real Number)

But this formula is not correct, because the sign of Imaginary Number or Real Number is not taken into account.



Take the A channel as a reference and change the Phase (via SPI) of channel B, C, D to have the same phase difference between each channel.

2nd Option for adjusting Phase:

After offset and gain calibration, only phase needs to be set.

If you look at the FTT graph, the set-up where the Phase is not calibrated creates an interleaving Spur (fundamental image spur). See Section 2.3 ”Phase Adjustment” on page 7.

Apply an analog sinus wave (Ex: 600.59 MHz sinus wave) and capture the output data for each ADC and interleave the data in this order A, C, B, D.

Calculate the FFT spectrum with interleaving data and calculate the FFT spectrum and calculate the power of each fundamental image spur.

Take the A channel as a reference and adjust the Phase (via SPI) of B channel to minimize this interleaving spur, when this value is minimized do the same adjustment for C and D channel. Repeat the same procedure B, C, D to minimize this interleaving spur.

When the interleaving spur is below the Harmonics spur, this process of adjusting for Phase can be considered acceptable for completing the calibration of the 4 channels.

3.4 Summary

Calibration of QUAD 8-bit is only needed only once and it is not necessary to perform a new calibration for each ADC power-up.

Calibration must be done with the highest frequency possible (around 600 MHz equal to the maximum frequency used in your system) for calibrate the phase of your system.

There is no need to repeat a new calibration versus analog input frequency.

It is recommended that calibration be performed at ambient temperature (ie. middle of the range of the temperature of your system). There is no need to repeat a new calibration versus temperature if the application operates in a ±20° C range.

Calibration needs be done at typical voltage. There is no need to repeat a new calibration versus power supplies.

Calibration needs to be done on each EV8AQ160CTPY device due to slight matching errors in Offset, Gain and Phase (delay) that are part to part dependant.

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