Comparison EV8AQ160 with EV10AQ190 ADC

Application Note

1. Introduction

This application note aims at providing you with a comparison between EV8AQ160 QUAD 8-bit and EV10AQ190 QUAD 10-bit.

It first compares the two versions including:

- Feature
- Pinout

It also describes board modifications to migrate from QUAD 8-bit to QUAD 10-bit.

2. Comparing EV8AQ160 and EV10AQ190 ADC Devices

The EV8AQ160 and EV10AQ190 are delivered in the same package, with same footprint and same mechanical parameters.

The EV10AQ190 and EV8AQ160 have been designed in order to feature the same timing characteristics.

The EV10AQ190 and EV8AQ160 have been designed in order to feature the same Power supplies.

The following section discusses the similarities and differences between the EV8AQ160 and the EV10AQ190.

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Figure 2-1. Simplified Block Diagram EV8AQ160

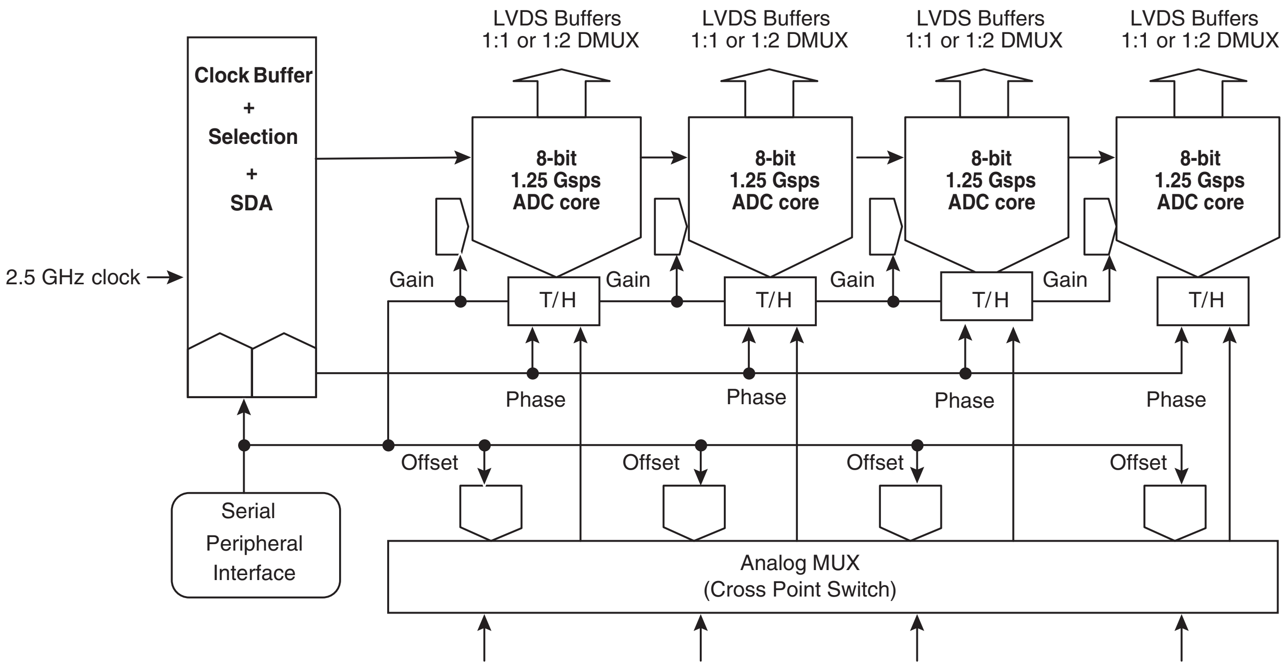
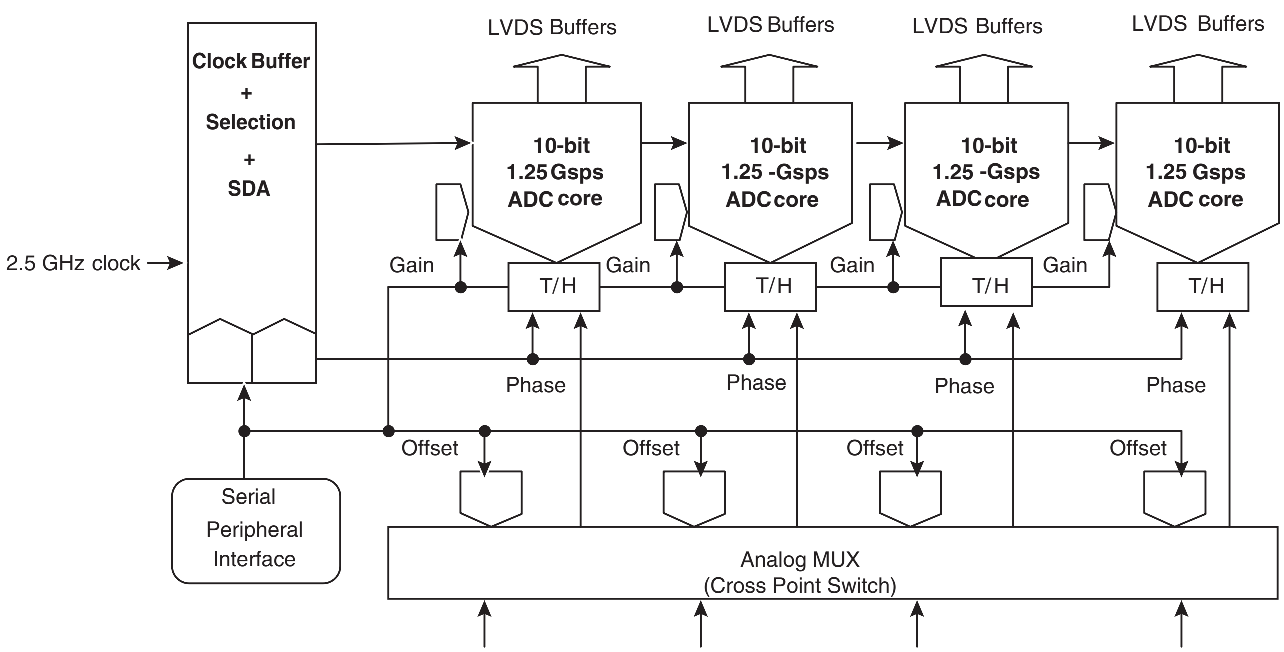


Figure 2-2. Simplified Block Diagram EV10AQ190



2.1 Comparison EV8AQ160 and EV10AQ190

Highlights of the differences between the two devices:

- Resolution
- DMUX output
- Three-digital control Gain Offset Phase
- Performance
- Flashing mode

Table 2-1. Features

EV8AQ160 Quad ADC with 8-bit Resolution	EV10AQ190 Quad ADC with 10-bit Resolution
Selectable 1:1 or 1:2 Demultiplexed Outputs	No DMUX
500 mVpp or 625 mVpp Analog Input (Differential input)	500 mVpp Analog Input (Differential input)
Selectable bandwidth (4 available settings)	Selectable bandwidth (2 available settings)
Offset Control (8-bit register) 256 steps	Offset Control (10-bit register) 1024 steps
Gain Control (8-bit register) 256 steps	Gain Control (10-bit register) 1024 steps
Gain Control (8-bit register) 256 steps	Phase Control (10-bit register) 1024 steps
Test mode with one Flashing mode with 7 FF pattern every eleven 00 patterns	Test mode with one Flashing mode with 7 FF pattern every eleven 00 patterns And added 2 Test modes: “Flashing 12” and “Flashing 16”, for which the period is respectively 12 or 16 in addition to the initial Flashing mode with period of 11

Highlights of the differences of performance between the two devices:

Table 2-2. Performance

EV8AQ160 Power Dissipation: 4.2 W Total (1:1 DMUX mode)	EV10AQ190 Power Dissipation: 5.8W Total
Input common mode 1.8V	Input common mode 1.6V
Full Power Input Bandwidth 2 GHz	Full Power Input Bandwidth: 3GHz
4-channel mode (Fsampling = 2.5 Gsps, –1 dBFS)	**4-channel mode (Fsampling = 2.5 Gsps, –1 dBFS)**
Fin = 100 MHz (minimum Bandwidth) ENOB = 7.5 bit, SFDR = 58 dBc, SNR = 46.5 dBc, DNL = ±0.18 LSB, INL = ±0.4 LSB	Fin = 100 MHz (Nominal Bandwidth): ENOB = 8.8 bit, SFDR = 65 dBc, SNR = 57 dB, DNL = ±0.3 LSB, INL = ±1.5 LSB
Fin = 620 MHz (Full Bandwidth): ENOB = 7.3 bit, SFDR = 56 dBc, SNR = 45 dBc	Fin = 620 MHz (Full Bandwidth): ENOB = 8.5 bit, SFDR = 63 dBc, SNR = 54 dB
	Fin = 1.2 GHz (Full Bandwidth): ENOB = 7.8 bit, SFDR = 57 dBc, SNR = 50 dB
2-channel mode (Fsampling = 2.5 Gsps, –1 dBFS) (after calibration)	**2-channel mode (Fsampling = 2.5 Gsps, –1 dBFS) (after calibration)**
Fin = 100 MHz (minimum Bandwidth) ENOB = 7.5 bit, SFDR = 58 dBc, SNR = 46 dBc, DNL = ±0.14 LSB, INL = ±0.35 LSB	Fin = 100 MHz (Nominal Bandwidth): ENOB = 8.7 bit, SFDR = 63 dBc, SNR = 56 dB, DNL = ±0.3 LSB, INL = ±1.5 LSB

Table 2-2. Performance (Continued)

EV8AQ160 **Power Dissipation: 4.2 W Total (1:1 DMUX mode)**	**EV10AQ190** **Power Dissipation: 5.8W Total**
Fin = 620 MHz: (Full Bandwidth): ENOB = 7.2 bit, SFDR = 56 dBc, SNR = 44.5 dBc	Fin = 620 MHz (Full Bandwidth): ENOB = 8.4 bit, SFDR = 61dBc, SNR = 54 dB
	Fin = 1.2 GHz (Full Bandwidth): ENOB = 7.7 bit, SFDR = 55 dBc, SNR = 50 dB
1-channel mode (Fsampling = 5 Gsps, –1 dBFS) (after calibration)	**1-channel mode (Fsampling = 5 Gsps, –1 dBFS) (after calibration)**
Fin = 100 MHz (minimum bandwidth) ENOB = 7.4 bit, SFDR = 58 dBc, SNR = 46 dBc, DNL = ±0.12 LSB, INL = ±0.27 LSB	Fin = 100 MHz (Nominal Bandwidth): ENOB = 8.7 bit, SFDR = 63 dBc, SNR = 56 dB, DNL = ±0.3 LSB, INL = ±1.5 LSB
Fin = 620 MHz: (Full bandwidth): ENOB = 7.1 bit, SFDR = 56 dBc, SNR = 44 dBc	Fin = 620 MHz (full bandwidth): ENOB = 8.4 bit, SFDR = 61 dBc, SNR = 54 dB
	Fin = 1.2 GHz (full bandwidth): ENOB = 7.7 bit, SFDR = 55 dBc, SNR = 50 dB

Table 2-3. TEST Register Description EV8AQ160

Bit label	Value	Description	Default Setting
TESTM	0	Increasing (simultaneous) ramp	0 Increasing ramp
	1	Flashing 1 (7 FF pattern every ten 00 patterns) on each ADC	

Table 2-4. TEST Register Description EV10AQ190

Bit label	Value	Description	Default Setting
TESTM	0	Increasing (simultaneous) ramp 11bit (0 up to 2047) see note 5	0 Increasing ramp
	1	Flashing mode (refer to Bit 1 and Bit 2 to select the flashing 1 period)	
FlashM	00	Flashing “11” mode = 1 (7 FF pattern every **ten** 00 patterns) on each ADC	00 Flashing “11” mode
	01	Flashing “12” mode = 1 (7 FF pattern every **eleven** 00 patterns) on each ADC	
	10	Flashing “16” mode = 1 (7 FF pattern every **fifteen** 00 patterns) on each ADC	

Notes:
1. TESTM is taken into account only if bit12 (TEST) of Control register (address 0x01) is at 1.
2. It is mandatory to apply a SYNCP, SYNCN signal to the ADC when the Test Mode is activated.
3. When Bit 0 is set to 1, it is necessary to choose the flashing “1” period (11, 12 or 16) using Bit 1 and Bit 2. The default flashing mode is the one with 11 period.
4. Flashing mode 7FF pattern on 11 bit (Out of range bit + data on 10-bit).
5. Ramp mode on 11 bit (Out of range bit + data on 10-bit).

2.2 Pinout EV8AQ160 and EV10AQ190

Figure 2-3. Pinout ADC QUAD 8-bit

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
AD	GND	VCC	BLD6	BLD7	BLOR	GND	DiodA	tdreadyp	tdcop	trigp	SYNCP	CLK	CLKN	scan0	scan2	sclk	mosi	Res50	GND	CLOR	CLD7	CLD6	VCC	GND
AC	GND	VCC	BLD6N	BLD7N	BLORN	GND	DiodC	tdreadyn	tdcon	trign	SYNCN	GND	GND	scan1	rstn	csn	miso	Res62	GND	CLORN	CLD7N	CLD6N	VCC	GND
AB	BHOR	BHORN	VCC	GND	VCC	GND	VCC	GND	GND	VCC	VCCD	GND	GND	VCC	VCC	GND	GND	VCC	GND	VCC	GND	VCC	CHORN	CHOR
AA	BHD7	BHD7N	VCC	GND	VCCO	VCC	VCC	GND	GND	VCC	VCCD	GND	GND	VCC	VCC	GND	GND	VCC	VCC	VCCO	GND	VCC	CHD7N	CHD7
Y	BHD6	BHD6N	VCCO	GND	GND	VCCO	VCC	GND	GND	VCC	VCCD	GND	GND	VCC	VCC	GND	GND	VCC	VCCO	GND	GND	VCCO	CHD6N	CHD6
W	BHD5	BHD5N	VCCO	GND	GND															GND	GND	VCCO	CHD5N	CHD5
V	BHD4	BHD4N	BLD5	BLD5N	GND															GND	CLD5N	CLD5	CHD4N	CHD4
U	BHD3	BHD3N	BLD4	BLD4N	VCCO															VCCO	CLD4N	CLD4	CHD3N	CHD3
T	BHD2	BHD2N	BLD3	BLD3N	GND															GND	CLD3N	CLD3	CHD2N	CHD2
R	BHD1	BHD1N	BLD2	BLD2N	VCC															VCC	CLD2N	CLD2	CHD1N	CHD1
P	BHD0	BHD0N	BLD1	BLD1N	GND															GND	CLD1N	CLD1	CHD0N	CHD0
N	BDR	BDRN	BLD0	BLD0N	VCC															VCC	CLD0N	CLD0	CDRN	CDR
M	ADR	ADRN	ALD0	ALD0N	VCC															VCC	DLD0N	DLD0	DDRN	DDR
L	AHD0	AHD0N	ALD1	ALD1N	GND															GND	DLD1N	DLD1	DHD0N	DHD0
K	AHD1	AHD1N	ALD2	ALD2N	VCC															VCC	DLD2N	DLD2	DHD1N	DHD1
J	AHD2	AHD2N	ALD3	ALD3N	GND															GND	DLD3N	DLD3	DHD2N	DHD2
H	AHD3	AHD3N	ALD4	ALD4N	VCCO															VCCO	DLD4N	DLD4	DHD3N	DHD3
G	AHD4	AHD4N	ALD5	ALD5N	GND															GND	DLD5N	DLD5	DHD4N	DHD4
F	AHD5	AHD5N	VCCO	GND	GND															GND	GND	VCCO	DHD5N	DHD5
E	AHD6	AHD6N	VCCO	GND	GND	VCCO	VCC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCCO	GND	GND	VCCO	DHD6N	DHD6
D	AHD7	AHD7N	VCC	GND	VCCO	VCC	VCC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCC	VCCO	GND	VCC	DHD7N	DHD7
C	AHOR	AHORN	VCC	GND	VCC	VCC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCC	GND	VCC	DHORN	DHOR
B	GND	VCC	ALD6N	ALD7N	ALORN	GND	GND	GND	GND	GND	GND	CMIRefA	CMIRefC	GND	GND	GND	GND	GND	GND	DLORN	DLD7N	DLD6N	VCC	GND
A	GND	VCC	ALD6	ALD7	ALOR	GND	AAI	AAIN	GND	BAI	BAIN	GND	GND	CAI	CAIN	GND	DAI	DAIN	GND	DLOR	DLD7	DLD6	VCC	GND

VCC=3.3V VCCO = 1.8V VCCD = 1.8V

Figure 2-4. Pinout ADC QUAD 10-bit

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
AD	GND	VCC	B8	B9	BOR	GND	DiodA	NC	GND	NC	SYNCP	CLK	CLKN	scan0	scan2	sclk	mosi	Res50	GND	COR	C9	C8	VCC	GND
AC	GND	VCC	B8N	B9N	BORN	GND	DiodC	GND	VCC	NC	SYNCN	GND	GND	scan1	rstn	csn	miso	Res62	GND	CORN	C9N	C8N	VCC	GND
AB	NC	NC	VCC	GND	VCC	GND	VCC	GND	GND	VCC	VCCD	GND	GND	VCC	VCC	GND	GND	VCC	GND	VCC	GND	VCC	NC	NC
AA	NC	NC	VCC	GND	VCCO	VCC	VCC	GND	GND	VCC	VCCD	GND	GND	VCC	VCC	GND	GND	VCC	VCC	VCCO	GND	VCC	NC	NC
Y	NC	NC	VCCO	GND	GND	VCCO	VCC	GND	GND	VCC	VCCD	GND	GND	VCC	VCC	GND	GND	VCC	VCCO	GND	GND	VCCO	NC	NC
W	NC	NC	VCCO	GND	GND															GND	GND	VCCO	NC	NC
V	NC	NC	NC	NC	GND															GND	NC	NC	NC	NC
U	B7	B7N	NC	NC	VCCO															VCCO	NC	NC	C7N	C7
T	B5	B5N	B6	B6N	GND															GND	C6N	C6	C5N	C5
R	B3	B3N	B4	B4N	VCC															VCC	C4N	C4	C3N	C3
P	B1	B1N	B2	B2N	GND															GND	C2N	C2	C1N	C1
N	BDR	BDRN	B0	B0N	VCC															VCC	C0N	C0	CDRN	CDR
M	ADR	ADRN	A0	A0N	VCC															VCC	D0N	D0	DDRN	DDR
L	A1	A1N	A2	A2N	GND															GND	D2N	D2	D1N	D1
K	A3	A3N	A4	A4N	VCC															VCC	D4N	D4	D3N	D3
J	A5	A5N	A6	A6N	GND															GND	D6N	D6	D5N	D5
H	A7	A7N	NC	NC	VCCO															VCCO	NC	NC	D7N	D7
G	NC	NC	NC	NC	GND															GND	NC	NC	NC	NC
F	NC	NC	VCCO	GND	GND															GND	GND	VCCO	NC	NC
E	NC	NC	VCCO	GND	GND	VCCO	VCC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCCO	GND	GND	VCCO	NC	NC
D	NC	NC	VCC	GND	VCCO	VCC	VCC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCC	VCCO	GND	VCC	NC	NC
C	NC	NC	VCC	GND	VCC	VCC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCC	GND	VCC	NC	NC
B	GND	VCC	A8N	A9N	AORN	GND	GND	GND	GND	GND	GND	CMIRefAB	CMIRefCD	GND	GND	GND	GND	GND	GND	DORN	D9N	D8N	VCC	GND
A	GND	VCC	A8	A9	AOR	GND	AAI	AAIN	GND	BAI	BAIN	GND	GND	CAI	CAIN	GND	DAI	DAIN	GND	DOR	D9	D8	VCC	GND

2.3 Pinout Differences Summary

Figure 2-5. Areas Were Changes Occur

Test Zone

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
AD	GND	VCC			BOR	GND	DiodA				SYNCP	CLK	CLKN	scan0	scan2	sclk	mosi	Res50	GND	COR			VCC	GND
AC	GND	VCC			BORN	GND	DiodC				SYNCN	GND	GND	scan1	rstn	csn	miso	Res62	GND	CORN			VCC	GND
AB			VCC	GND	VCC	GND	VCC	GND	GND	VCC	VCCD	GND	GND	VCC	VCC	GND	GND	VCC	GND	VCC	GND	VCC		
AA			VCC	GND	VCCO	VCC	VCC	GND	GND	VCC	VCCD	GND	GND	VCC	VCC	GND	GND	VCC	VCC	VCCO	GND	VCC		
Y			VCCO	GNDO	GNDO	VCCO	VCC	GND	GND	VCC	VCCD	GND	GND	VCC	VCC	GND	GND	VCC	VCCO	GNDO	GNDO	VCCO		
W			VCCO	GNDO	GNDO															GNDO	GNDO	VCCO		
V					GNDO															GNDO				
U					VCCO															VCCO				
T					GND															GND				
R					VCC															VCC				
P					GND															GND				
N	BDR	BDRN			VCC															VCC			CDRN	CDR
M	ADR	ADRN			VCC															VCC			DDRN	DDR
L					GND															GND				
K					VCC															VCCA				
J					GND															GND				
H					VCCO															VCCO				
G					GNDO															GNDO				
F			VCCO	GNDO	GNDO															GNDO	GNDO	VCCO		
E			VCCO	GNDO	GNDO	VCCO	VCC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCCO	GNDO	GNDO	VCCO		
D			VCC	GND	VCCO	VCC	VCC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCC	VCCO	GND	VCC		
C			VCC	GND	VCC	VCC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC	VCC	GND	VCC		
B	GND	VCC			AORN	GND	GND	GND	GND	GND	GND	CMIRefAB	CMIRefCD	GND	GND	GND	GND	GND	GND	DORN			VCC	GND
A	GND	VCC			AOR	GND	AAI	AAIN	GND	BAI	BAIN	GND	GND	CAI	CAIN	GND	DAI	DAIN	GND	DOR			VCC	GND

Output Data Zone

Table 2-5. Migration EV8AQ160 to EV10AQ190

Port A		Port B		Port C		Port D	
EV8AQ160	**EV10AQ190**	**EV8AQ160**	**EV10AQ190**	**EV8AQ160**	**EV10AQ190**	**EV8AQ160**	**EV10AQ190**
AL0	A0	BL0	B0	CL0	C0	DL0	D0
AL0N	A0N	BL0N	B0N	CL0N	C0N	DL0N	D0N
AH0	A1	BH0	B1	CH0	C1	DH0	D1
AH0N	A1N	BH0N	B1N	CH0N	C1N	DH0N	D1N
AL1	A2	BL1	B2	CL1	C2	DL1	D2
AL1N	A2N	BL1N	B2N	CL1N	C2N	DL1N	D2N
AH1	A3	BH1	B3	CH1	C3	DH1	D3
AH1N	A3N	BH1N	B3N	CH1N	C3N	DH1N	D3N
AL2	A4	BL2	B4	CL2	C4	DL2	D4
AL2N	A4N	BL2N	B4N	CL2N	C4N	DL2N	D4N
AH2	A5	BH2	B5	CH2	C5	DH2	D5
AH2N	A5N	BH2N	B5N	CH2N	C5N	DH2N	D5N
AL3	A6	BL3	B6	CL3	C6	DL3	D6
AL3N	A6N	BL3N	B6N	CL3N	C6N	DL3N	D6N
AH3	A7	BH3	B7	CH3	C7	DH3	D7
AH3N	A7N	BH3N	B7N	CH3N	C7N	DH3N	D7N
AL6	A8	BL6	B8	CL6	C8	DL6	D8
AL6N	A8N	BL6N	B8N	CL6N	C8N	DL6N	D8N
AL7	A9	BL7	B9	CL7	C9	DL7	D9
AL7N	A9N	BL7N	B9N	CL7N	C9N	DL7N	D9N
AL0R	A0R	BL0R	B0R	CL0R	C0R	DL0R	D0R
ALORN	AORN	BLORN	BORN	CLORN	CORN	DLORN	DORN
ADR	ADR	BDR	BDR	CDR	CDR	DDR	DDR
ADRN	ADRN	BDRN	BDRN	CDRN	CDRN	DDRN	DDRN

Table 2-6. Test Pin Comparaison

EV8AQ160		EV10AQ190	
AD8	GND	AD8	NC
AC8	GND	AC8	GND
AD9	NC	AD9	GND
AC9	10 KΩ to GND	AC9	VCC
AD10	NC	AD10	NC
AC10	NC	AC10	NC

AD8: connect to GND or leave no connect for both EV8AQ160 and EV10AQ190.

AD9: connect to GND or leave no connect for both EV8AQ160 and EV10AQ190.

AC9: must be connected to VCC for EV10AQ190 device to have an optimum performance

AC9: must be connected to 10 KΩ to GND or GND for EV8AQ160 device to have an optimum performance.

Jumper could be soldered, in order to replace easily the QUAD8-bit by the QUAD10-bit configuration

or this configuration could be driven by FPGA.

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