Application Note

1. Introduction

The aim of this application is to provide you with some recommendations to implement the EV8AQ160 Quad 8-bit 1.25 Gsps ADC in your system.

It first presents the ADC input/output interfaces and then provides some recommendations in regards to the device settings and board layout in order to obtain the best performance of the device. This document applies to the EV8AQ160 8-bit 1.25 Gsps ADC.

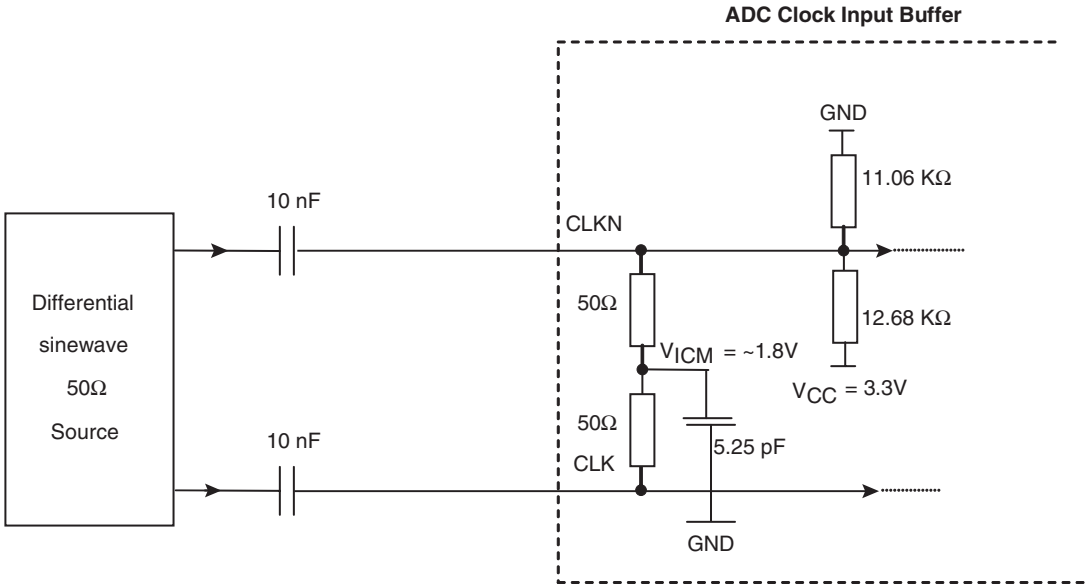
2. EV8AQ160 ADC Input Terminations

2.1 Clock Input

It is recommended to drive the Quad ADC input clock in a differential mode in order to optimize the performance of the ADC and minimize the injection of noise in the die ground plane.

As the clock input common mode is 1.8V, it is recommended to AC couple the clock signal, as illustrated in Figure 2-1.

Figure 2-1. EV8AQ160 ADC Clock Input Termination Scheme



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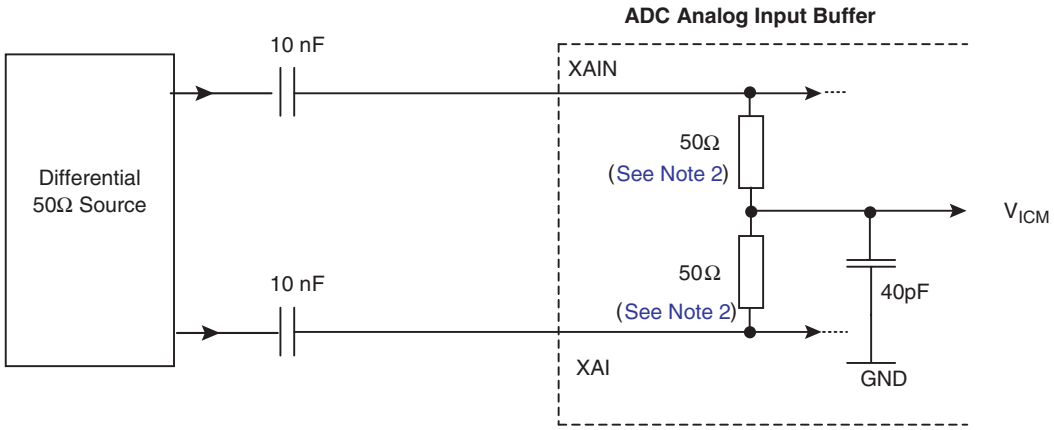
2.2 Analog Input

e2v recommends analog input (any channel) in differential mode. A balun can be used in order to convert a single-ended source to a differential signal at the input of ADC (see e2v for details).

2.2.1 Differential Analog Input

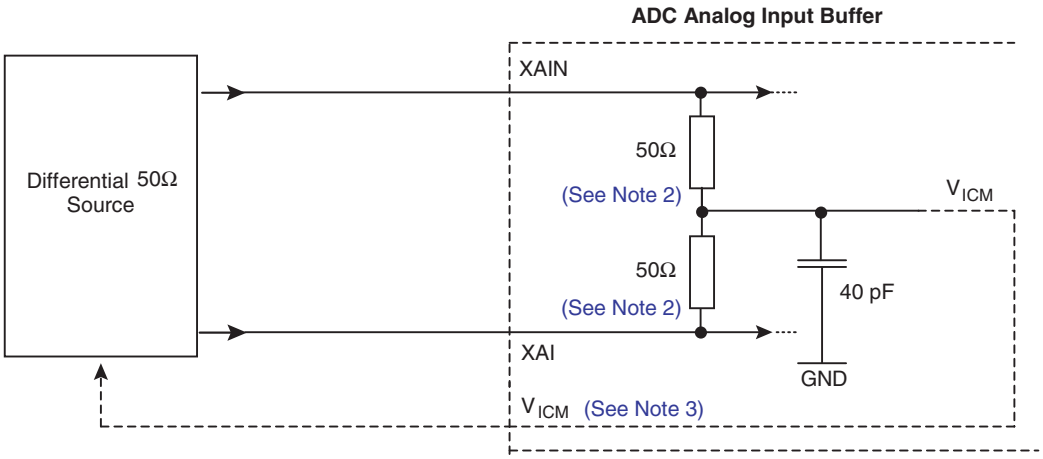
The analog input can be either DC or AC coupled as described in Figure 2-2 and Figure 2-3.

Figure 2-2. Differential Analog Input Implementation (AC Coupled)



Notes:
1. X = A, B, C or D.
2. The 50Ω terminations are implemented on-chip and can be fine tuned (TRIMMER register at address 0x13).
3. V_{ICM} = 1.8V.

Figure 2-3. Differential Analog Input Implementation (DC Coupled)



Notes:
1. X = A, B, C or D.
2. The 50Ω terminations are implemented on-chip and can be fine tuned (TRIMMER register at address 0x13).
3. V_{ICM} = 1.8V. The VICM signal is output from the ADC to provide the common mode to the front-end.

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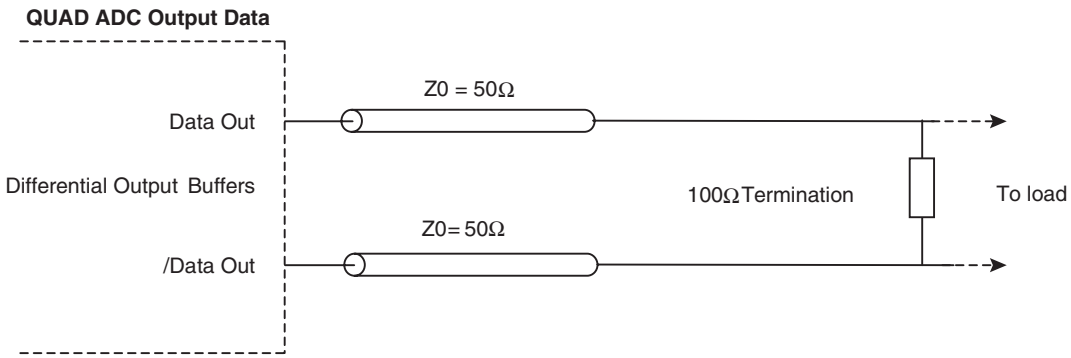
3. EV8AQ160 ADC Output Terminations

The digital outputs are LVDS compatible. They have to be 100Ω differentially terminated.

Figure 3-1. Differential Digital Outputs Terminations (100Ω LVDS)



4. EV8AQ160 ADC Hardware Signals

4.1 RESET Signals

4.1.1 ADC Synchronization Signal (SYNC, SYNCN)

The SYNC, SYNCN signal has LVDS electrical characteristics. It is active high and should last at least 2 clock cycles to work properly.

Once set at high level, it has an effect on the output clock signals which are then forced to LVDS low level as described in Figure 4-1 on page 4. During reset, the output data is not refreshed.

Once reset at low level, the output clock signals restart toggling after (TDR + pipeline delay) + Y clock cycles, where Y can be selected via the Serial Peripheral Interface at address 0x06 (from 0 to 15).

This SYNC signal can be used to ensure the synchronization of multiple ADCs.

Note: In DMUX 1:2 mode, the SYNC, SYNCN signal also resets the clock divider for the DMUX.

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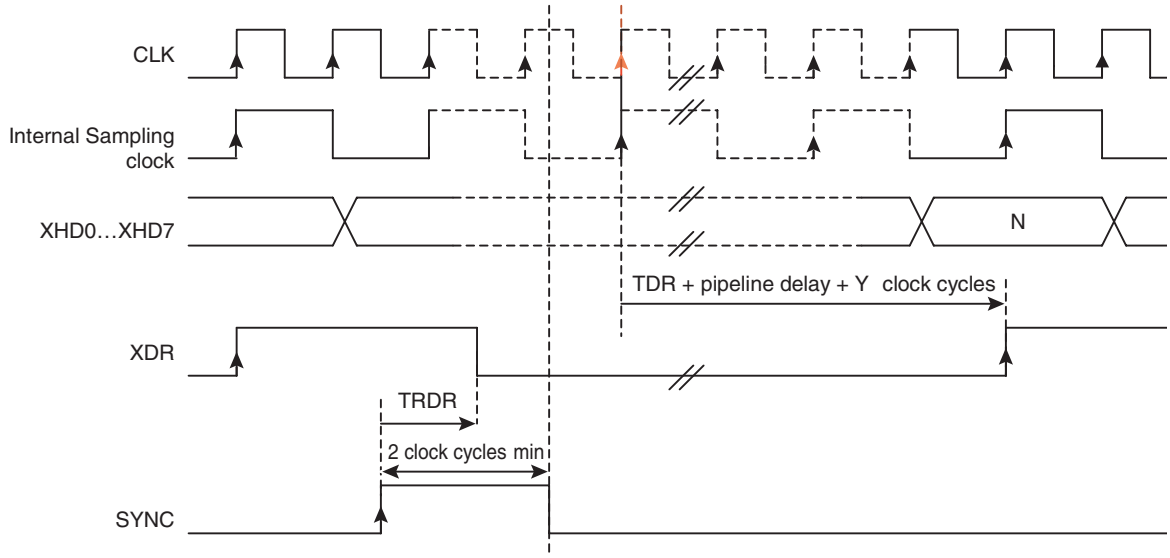
Figure 4-1. SYNC Timing in Four-channel Mode, 1:1 DMUX Mode (for Each Channel)



Note: X refers to A, B, C and D.

4.1.2 Digital Reset (RSTN)

This is a global hardware Reset of SPI register. It is active low.

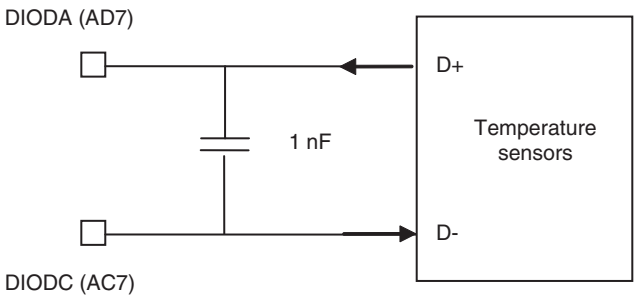
Notes: 1. There are two methods to reset the Quad 8-bit 1.25 Gsps ADC:
2. By asserting low the RSTN primary pad (hardware reset)
3. By writing a “1” in the bit SWRESET of the SWRESET register through the SPI (software reset)

Both methods will clear all configuration registers to their reset values.

4.2 DIODE

DIODEA, DIODEC: two pins are provided so that the diode can be probed using standard temperature sensors.

Figure 4-2. Junction Temperature Monitoring Diode System



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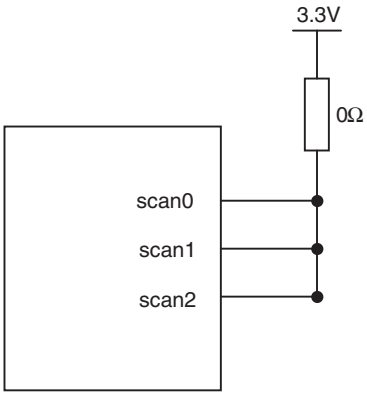
4.3 SCAN Signals

The scan signals (pins AD14, AC14, AD15) should be connected to 3.3V as illustrated in Figure 4-3.

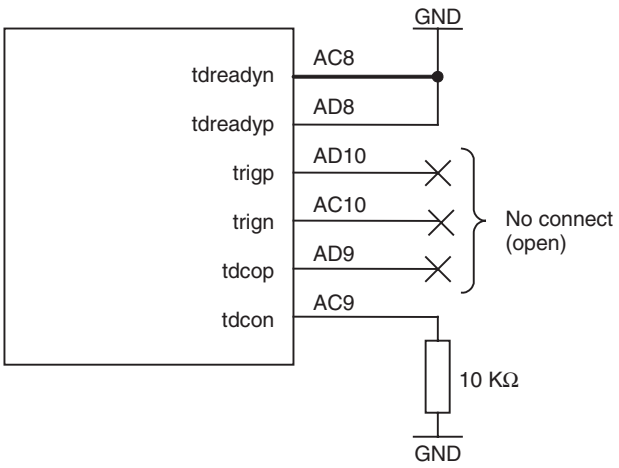
Figure 4-3. Scan Signals Recommended Implementation



4.4 Test Signals

The reserved signals (trigp pin AD10, trign pin AC10, tdreadyp pin AD8, tdreadyn pin AC8, tdcop pin AD9 and tdcon pin AC9) should be connected as described in Figure 4-4.

Figure 4-4. Reserved Pins Recommended Implementation



5. SPI

Atmel ATmega128L VR can be used to drive the SPI port of the EV10AQ190 Quad 10-bit 1.25 Gsps ADC.

In this first section, a simple configuration for the interfacing of the AVR with the ADC is provided.

Note: All the information contained in this document concerning the AVR complies with the version available at the date the document was created. It should be checked versus the current version available before design.

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5.1 EV8AQ160 8-bit 1.25 Gsps ADC SPI

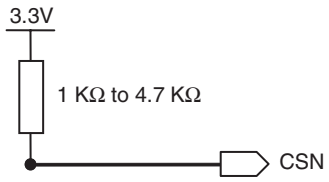
Five signals of the EV8AQ160 Quad 8-bit 1.25 Gsps ADC can be driven via the ATmega128L AVR:

- The CSN signal (pin AC16): used in the ADC to activate the 3-wire serial interface
- The SCLK signal (pin AD16): input clock for the SPI
- The MISO signal (pin AC17): master input slave output of the SPI (output of the ADC)
- The MOSI signal (pin AD17): master output slave input of the SPI (input for the ADC)
- The RSTN signal (pin AC15): external reset for the SPI

5.1.1 CSN Signal

This signal should be pulled up to V_{CC} = 3.3V via a pull-up resistor (1 KΩ to 4.7 KΩ) if it is not used, so that it is not activated by default.

Figure 5-1. CSN Implementation if not use



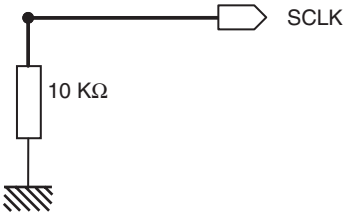
This signal could be connected directly to FPGA or Micro controller like FX2 or AVR if it is used.

Figure 5-2. CSN Implementation if use

5.1.2 SCLK Signal

This signal should be pulled down to ground via a 10 KΩ resistor if not use, so that it is not activated by default.

Figure 5-3. SCLK Implementation if not use



This signal could be connected directly to FPGA or Micro controller if it is used.

Figure 5-4. SCLK Implementation if use

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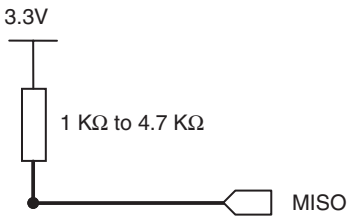
5.1.3 MISO Signal

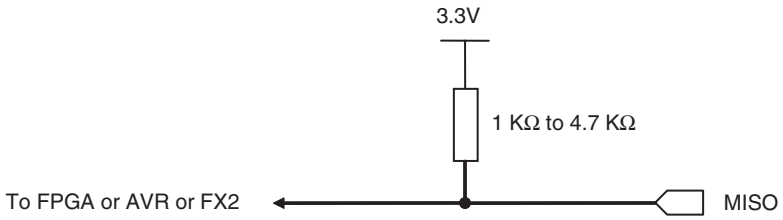
This signal must be pulled up to V_{CC} = 3.3V via a pull-up resistor (1 KΩ to 4.7 KΩ) **if it is used or not** so that it is not activated by default.

Figure 5-5. MISO Implementation if not use



This signal must be pulled up to V_{CC} = 3.3V via a pull-up resistor (1 KΩ to 4.7 KΩ) even if it is used.

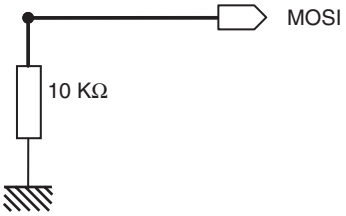
Figure 5-6. MISO Implementation if use



5.1.4 MOSI Signal

This signal should be pulled down to ground via a 10 KΩ resistor if it not used so that it is not activated by default.

Figure 5-7. MOSI Implementation if not use



This signal could be connected directly to FPGA or Micro controller like FX2 or AVR if it is used.

Figure 5-8. MOSI Implementation if use

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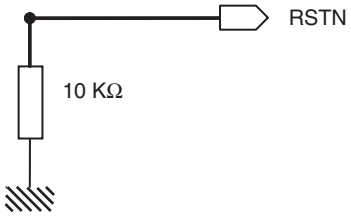
5.1.5 RSTN Signal

This signal should be pulled down to GND via a 10 KΩ resistor, if it is used so that it is activated by default and the default parameters will apply.

Figure 5-9. RSTN Implementation (Command via the AVR and via a Push Button) if not use

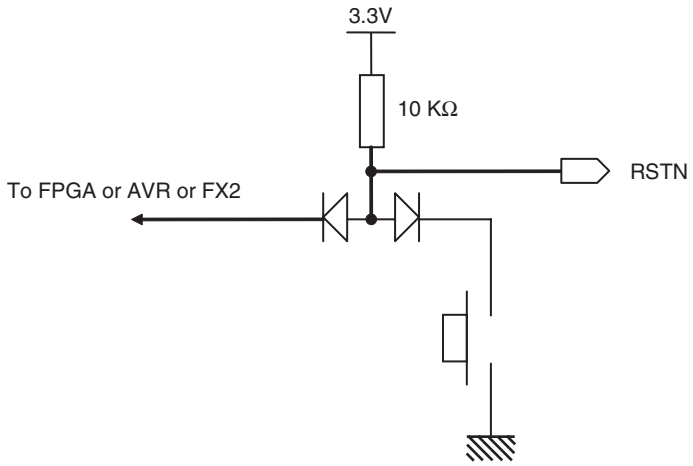


This signal could be connected directly to FPGA or Micro controller like FX2 or AVR if it is used.

Figure 5-10. RSTN Implementation if use

As this reset is normally a hardware reset, it can be useful to allow an external reset by a push button for example. In order to work out the conflict between the AVR and the push button, diodes can be used as illustrated in Figure 5-1 on page 6.

Figure 5-11. RSTN Implementation (Command via the AVR and via a Push Button)



5.1.6 Systems with Multiple SPI Slaves

Since the MISO output does not conform to the SPI standard in systems with multiple SPI slaves it is necessary to buffer the SPI signals..

This can be done using a 74LVC1T45 transceiver which can also be used to translate between different voltage levels.

The figure below shows a typical system where the Micro takes the role of SPI master and so the MISO signal will be an input.

The ADC requires a pull-up of around 1KOhm on its output which is then input to the buffer translator 74LVC1T45. The DIR input of this device can be used by the SPI chip select signal from the Micro to disconnect the output from the common SPI line.

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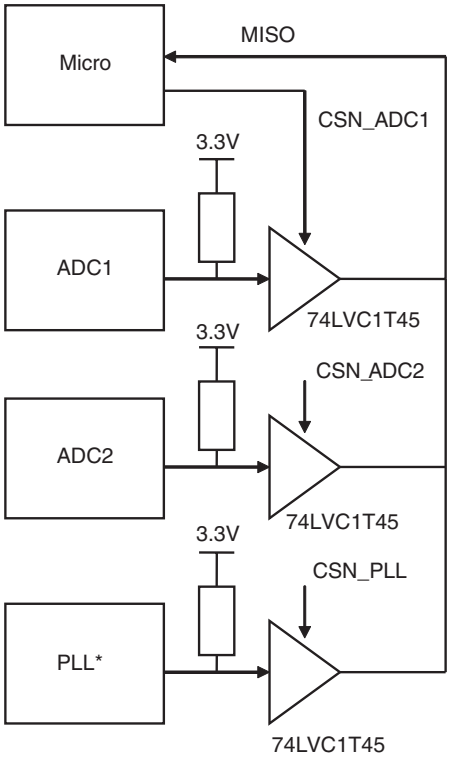
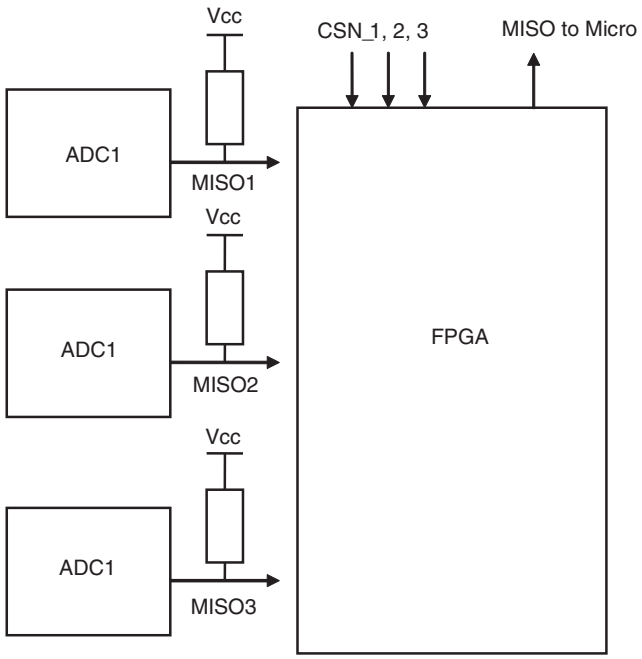
A similar technique should be used for other SPI peripherals on the bus if required.

Figure 5-12. SPI System with Multiple Slaves



Note: if MOSI used.

Figure 5-13. SPI System with Multiple Slaves Using FPGA as Buffer



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5.1.7 ATmega128L 8-bit Microcontroller In-System Programmable Flash

Because Port B provides the pins for the SPI channel, this is the port chosen for the four signals of the ADC SPI as well as the RSTN signal:

- CSN to PB4 (OC0 = Output Compare and PWM Output for Timer/Counter0)
- SCLK to PB1 (SCK = SPI bus serial clock)
- MOSI to PB2 (MOSI = SPI bus Master Output/Slave Input)
- MISO to PB3 (MISO = SPI bus Master Input /Slave Output)
- RSTN to PB5 (OC1A = Output Compare and PWM Output A for Timer/Counter1)

The other pins PB0 ($\overline{SS}$), PB6 (OC1B) and PB7 (OC2/OC1C) can be left floating (open).

Pin PB3 (MISO = SPI Bus Master Input/Slave Output) needs to be pulled up to 3.3V via a 1 kΩ resistor in order to be forced to a high level and not left open.

Pins SPICLOCK = PB1 and SPIDATA = PB2 need to be pulled down to ground via a 10 kΩ resistor to be forced to low level (inhibition of the SPI during reset of the microcontroller).

Pin SLE = PB4 (OC0 = Output Compare and PWM Output for Timer/Counter0) needs to be pulled up to 3.3V via a 3.3 kΩ (or 1 kΩ if the power consumption is not critical) resistor in order to protect the line during reset of the microcontroller (in which phase the signal becomes an input).

Ports A and C of the AVR can be left floating (open) but have to be internally configured with pull-ups.

For Port D, pins PD7, PD6, PD5 and PD4 can be left unused (open) but have to be internally configured with pull-ups. Pins PD3, PD2, PD1 and PD0 have to be pulled up to 3.3V via a 1 kΩ resistor in order to inhibit external interrupts.

For port E, pins PE3 and PE2 can be left unused (open) but have to be internally configured with pull-ups. Pins PE7, PE6, PE5 and PE4 have to be pulled up to 3.3V via a 1 kΩ resistor in order to inhibit external interrupts.

PE1 and PE0 can be used as the Programming Data Output (TX) and Input (RX) to be connected to the TX and RX of the system (in the case of the EV8AQ160-EB evaluation board, these signals are sent to the PC via an RS232 port).

All the pins of Port F have to be connected to ground so that they are in a known fixed state (no internal pull-down available for these pins).

All pins of Port G can be left floating (open).

Finally, the five remaining signal pins are to be connected as follows:

- $\overline{PEN}$ = programming enable pin for the SPI serial programming mode, to be connected to V_{CC} = 3.3V to activate the SPI programming mode
- $\overline{RESET}$ = Master reset of the AVR, to be connected to a microcontroller supervisory circuit (for example and for information only: MCP809 from Microchip™, one possible configuration is given in the next section)
- XTAL1 and XTAL2: input and output to/from the inverting oscillator amplifier
- AREF = analog reference for the A/D internal converter

Finally, V_{CC} and A_{VCC} have to be connected to a 3.3V source and GND, to ground.

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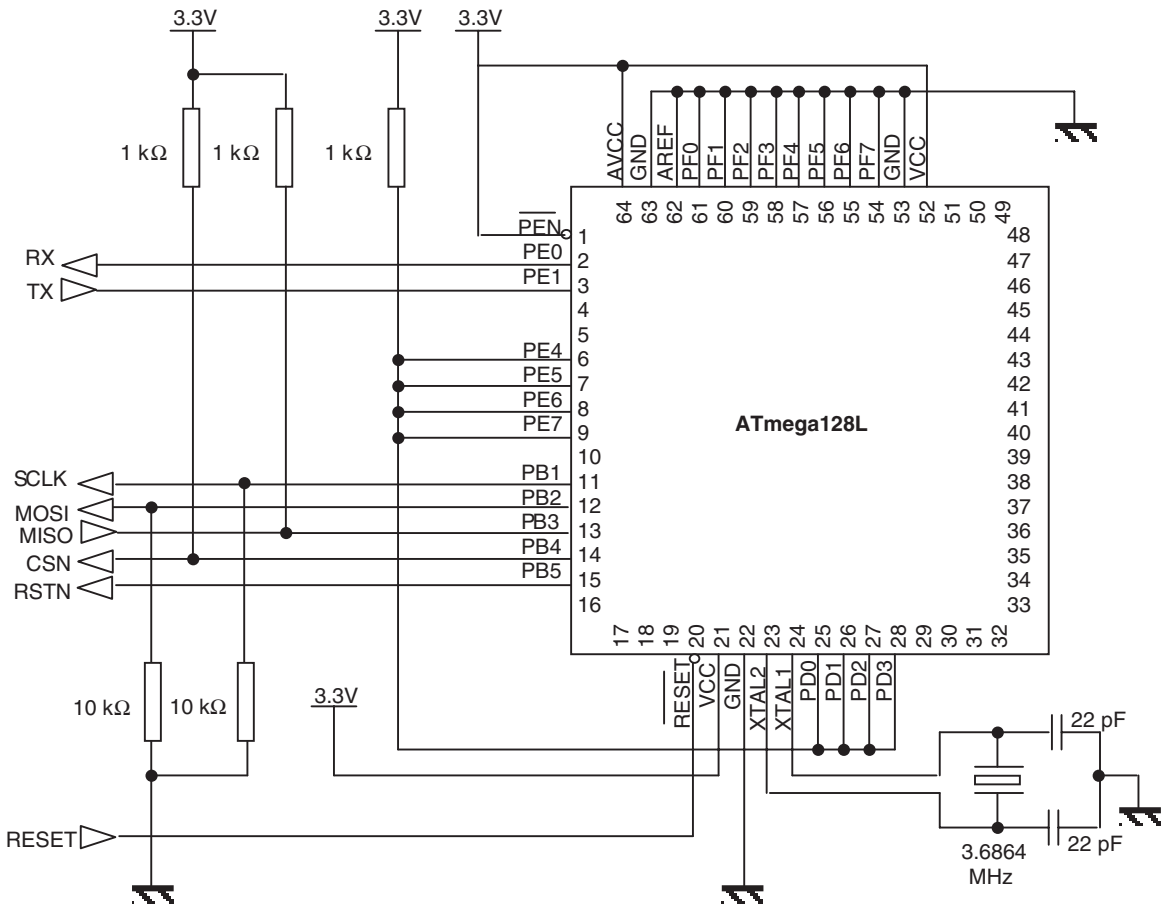
This gives the following configuration as described in Figure 5-14 (AVR only).

Figure 5-14. ATmega128L Application Diagram (for Use with e2v EV8AQ160 Quad 8-bit 1.25 Gsps ADC)



Note: Only the connected pins are shown (the unused pins are left open).

The reset of the ATmega128L AVR can be controlled thanks to a *voltage supervisory circuit* comparable to the MCP809 device from Microchip (for information only). Such a device allows you to keep the microcontroller in reset until the system voltage has reached its final level. It also ensures that the microcontroller will be reset whenever a power drop occurs.

Any voltage supervisory circuit compliant with V_{CC} = 3.3V and with a reset pulse longer than 50 ns minimum width (active low) would work.

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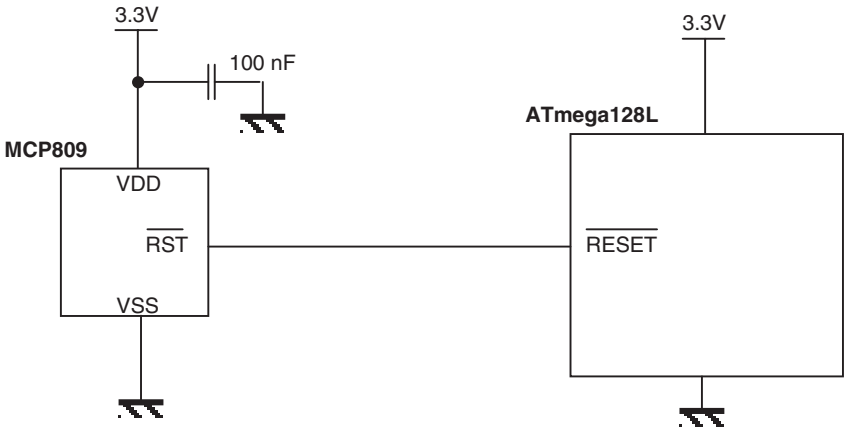
In Figure 5-15, the supervisory device from Microchip reset voltage level is set to 3.0V with a pulse of 350 ms.

Figure 5-15. Typical Application Diagram for the Circuit



5.2 Programming of Atmel ATmega128L AVR

Atmel ATmega128L AVR can be programmed thanks to the AVR ISP (In-System Programmer) tool using AVR Studio®, Atmel's Integrated Development Environment (IDE) for code writing and debugging. The programming software can be controlled from both Windows environment and a DOS command-line interface.

For more information on the AVR Studio programming software, please refer to Atmel Website.

The programming of the AVR requires the use of a 6-pin or 10-pin ISP connector.

In our case, an HE10 6-pin connector is chosen:

- Pin 1 = PDO, AVR Programming Data Out
- Pin 2 = AVR target application card power supply (= 3.3V)
- Pin 3 = SCK, AVR programming clock
- Pin 4 = PDI, AVR Programming Data In
- Pin 5 = RST_ISP, AVR programming Reset
- Pin 6 = ground

Notes: 1. The ISP card power supply comes from the AVR card (3.3V). There is no need for an additional power supply.

2. The mode used to program the AVR is a serial mode.

The RST_ISP signal is used to manage the AVR mode: programming mode or SPI mode.

This signal is sent to the $\overline{\text{RESET}}$ of the AVR so that:

- When RST_ISP = 0, $\overline{\text{RESET}}$ = 0 and the AVR is in reset (ISP mode), PE0 is used as the Data In for the programming of the AVR, PE1 is the Data Out and PB1 is the programming clock
- When RST_ISP = 1, $\overline{\text{RESET}}$ = 1 and the AVR is in normal mode, PE0 = RX, PE1 = TX, PB1 = SCLK

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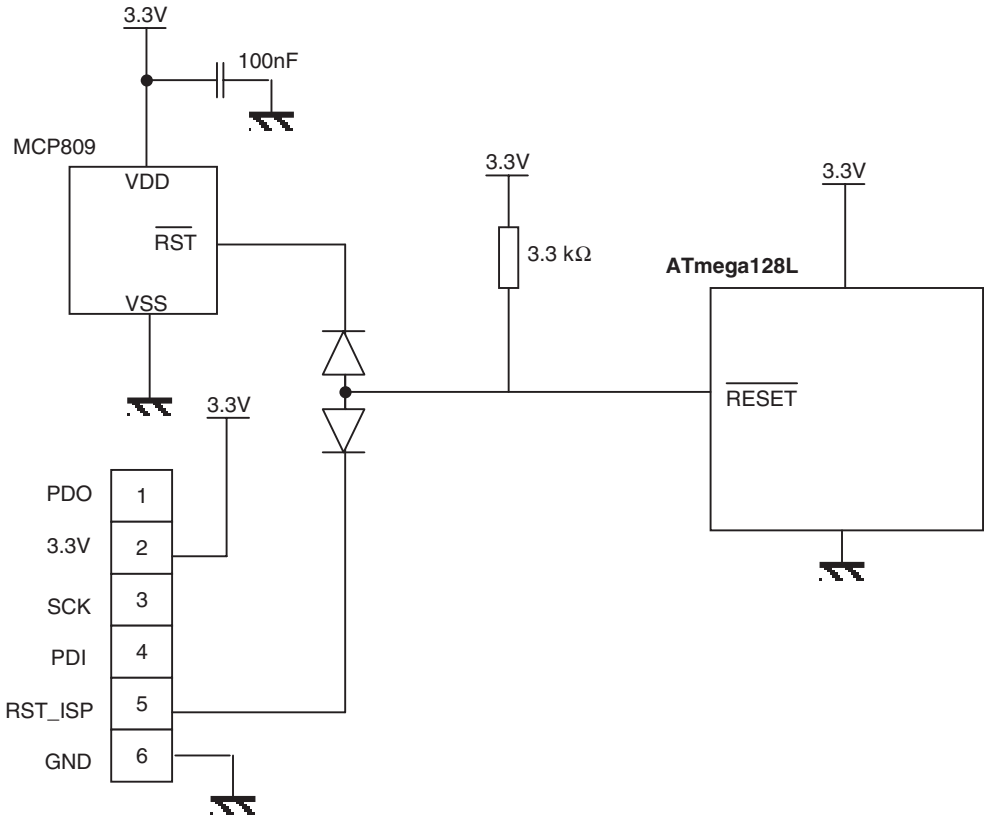
The three AVR signals mentioned previously (PE0, PE1 and PB1) thus, have two functions controlled by RST_ISP. Be careful when implementing these signals series resistors on the SCK, PDO and PDI data may be needed to manage possible conflicts, see Section 6.

Similarly, the $\overline{\text{RESET}}$ signal has two possible sources: the signal generated by the microcontroller supervisory device and the RST_ISP signal from the ISP. In order to manage this signal and in case the microcontroller supervisory device is not with open collector (as for the MCP809 device), two head-to-tail diodes are required, as illustrated in Figure 5-16. The line going to the $\overline{\text{RESET}}$ signal of the AVR is then in open-collector and a pull-up resistor (3.3 kΩ) to 3.3V is required.

Figure 5-16. Typical Application Diagram for the Circuit with the ISP Connector



A basic diagram illustrating the interface between the ISP connector and the AVR is depicted in Figure 5-17 on page 14. In this general case, PE1 and PE0 interconnections are left to the user's responsibility. In case of possible conflict on these signals (example PE1 could be driven by both PDO and another signal), it may be necessary to add a 1 kΩ resistor in series so that any voltage difference will be dissipated in this resistor.

No additional protection is required on the AVR PB1 signal as there is no conflict between SCLK and SCK. It is nevertheless recommended to set the ADC in standby mode or disable the SPI thanks to the CSN bit during programming of the AVR.

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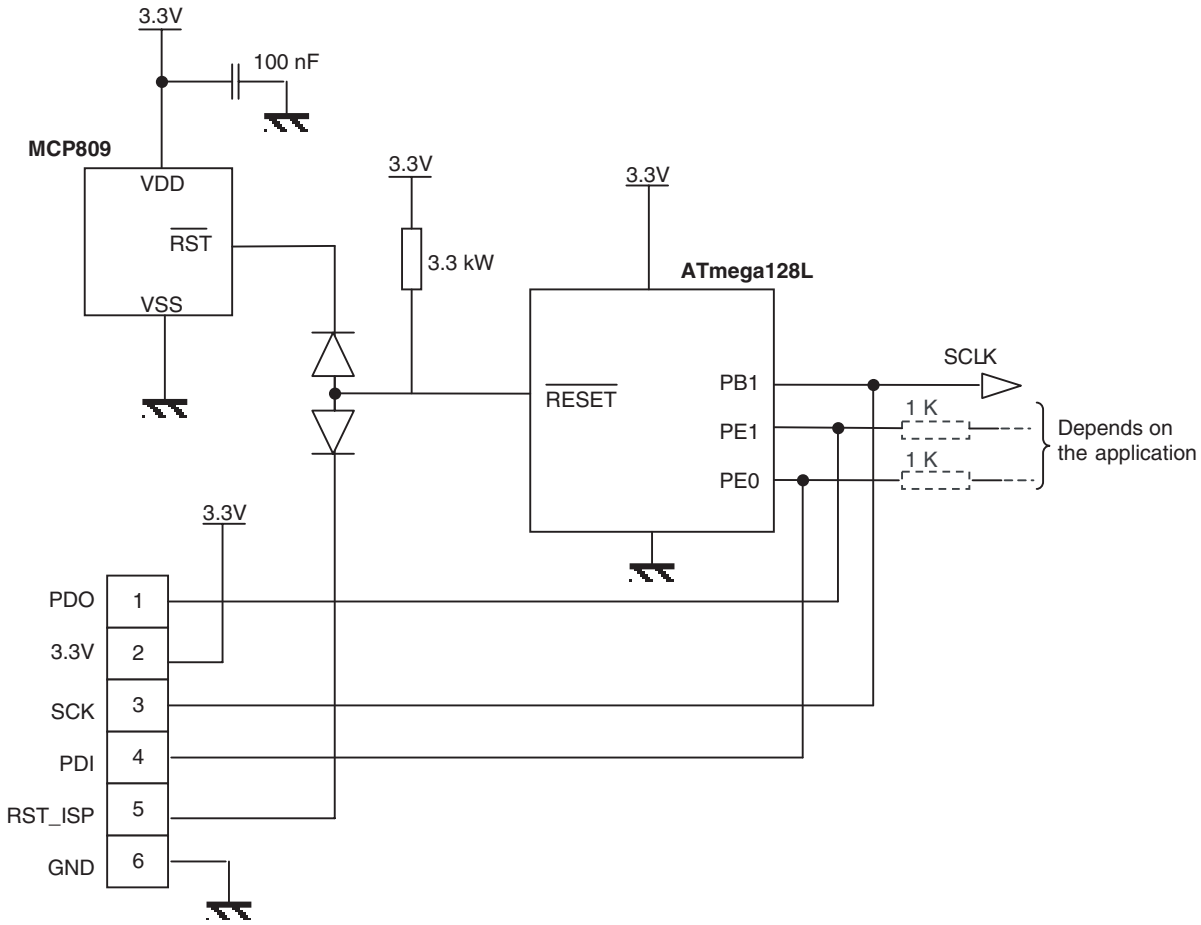
Figure 5-17. General Application Diagram for the ISP Connector and the AVR



In case the RX and TX signals are to be connected to a transceiver (RS232 connector to a PC for example), in order to multiplex the signals of the AVR (PE0, PE1 and PB1) between the ISP and the RX, TX and SCLK signals, a low voltage buffer/line driver with 3-state outputs device can be used. The 74LVQ241 devices are well-suited for this application (clock driver and bus oriented transmitter or receiver).

The 74LVQ241 device has eight inputs and eight corresponding outputs and two 3-state output enable inputs. These two 3-state output enable inputs can be managed by the RST_ISP signal:

- When RST_ISP = 0, $\overline{OE1}$ = OE2 = 0 and then O_0 to O_3 are low and O_4 to O_7 are in high impedance
- When RST_ISP = 1, $\overline{OE1}$ = OE2 = 1 and then O_0 to O_3 are in high impedance and O_4 to O_7 are low

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The truth table of the 74LVQ241 device is shown in Table 5-1.

Table 5-1. 74LVQ241Truth Table

Inputs		**Outputs** (O_0, O_1, O_2, O_3)
OE1	I_n	
L	L	L
L	H	H
H	X	Z
Inputs		**Outputs** (O_4, O_5, O_6, O_7)
OE2	I_n	
L	X	Z
H	L	L
H	H	H

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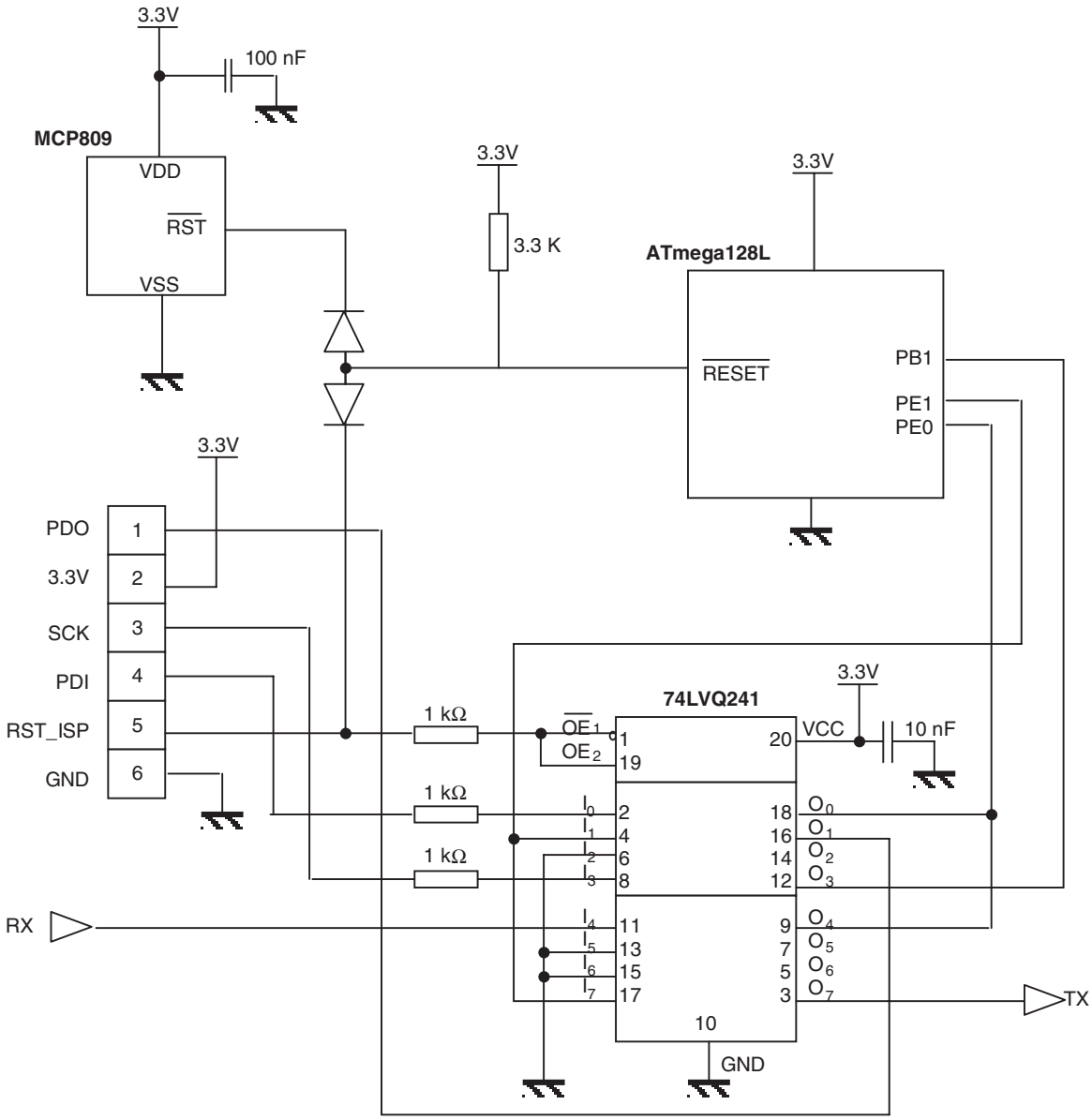
Figure 5-18. Typical Application Diagram with the 74LVQ241



Notes:
1. The unused inputs are connected to ground to prevent them from toggling.
2. $\overline{OE1}$ and OE2 are connected together and to RST_ISP via a 1 kΩ resistor.
3. SCK, RST-ISP and PDI are connected to I_3, $\overline{OE1}$ and OE2 and I0 respectively via 1 kΩ resistors in order to manage the possible conflicts on the signals in case the connector is used to program several AVRs.
4. PE0 is connected to both O_0 and O_4, which are respectively the inputs corresponding to SCK and RX: PE0 will be either generated by SCK or RX depending on the mode.
5. PE1 is connected to both I_1 and I_7, which are respectively the outputs corresponding to PDO and TX: PE1 will either generate by PDO or TX depending on the mode.

The programming of the AVR itself as well as the connections of the RX and TX signals are not described in this application note as they depend on the final application.

For more information on the AVR, please contact the AVR hotline at avr@atmel.com.

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6. Grounding and Power Supplies

6.1 Ground Plane

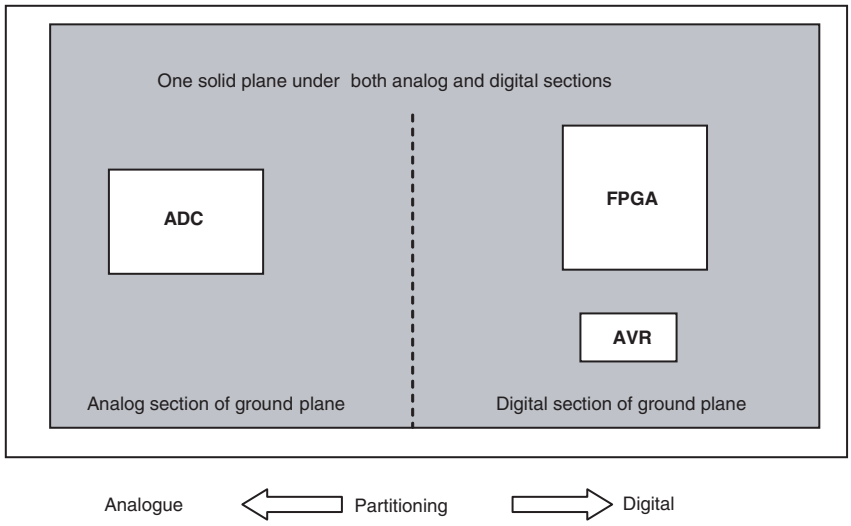
It is recommended to use the same common ground plane for the ADC, and the digital ground plane used for the digital part of the system (FPGA for example).

- Do not split the ground plane, use one solid plane under both analogue and digital sections of the board, see Figure 6-1).

Partition your PCB with separate analog and digital sections. Locate all analogue components and lines over the analogue power plane and all digital components and lines over the digital power plane.

Note: We recommend a minimum distance of 2 cm between the ADC and FPGA

Figure 6-1. Schematic View of The System Board Ground Plane (Example)



6.2 Power Supply Planes

The Quad ADC requires three distinct power supplies:

V_{CC} = 3.3V (for the analog parts and the SPI pads)

V_{CCD} = 1.8V (for the digital parts)

V_{CCO} = 1.8V (for the output buffers)

It is recommended to decouple all power supplies to ground as close as possible to the device balls with 220 pF in parallel to 33 nF capacitors. The minimum number of decoupling pairs of capacitors can be calculated as the minimum number of groups of neighboring pins.

17 capacitors of 220 pF and 8 capacitors of 33 nF for V_{CC}

8 capacitors of 220 pF and 4 capacitors of 33 nF for V_{CCO} and

1 capacitor of 220 pF and 1 capacitor of 33 nF for V_{CCD}

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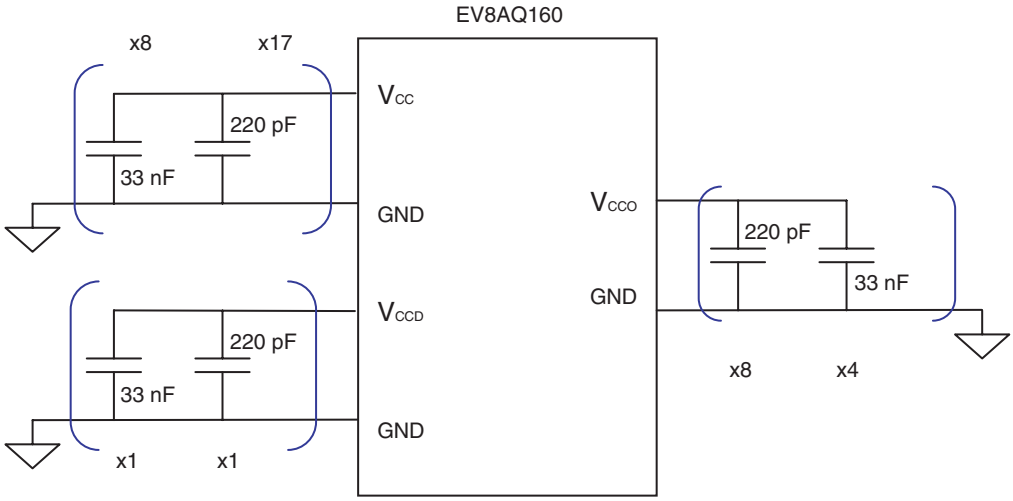
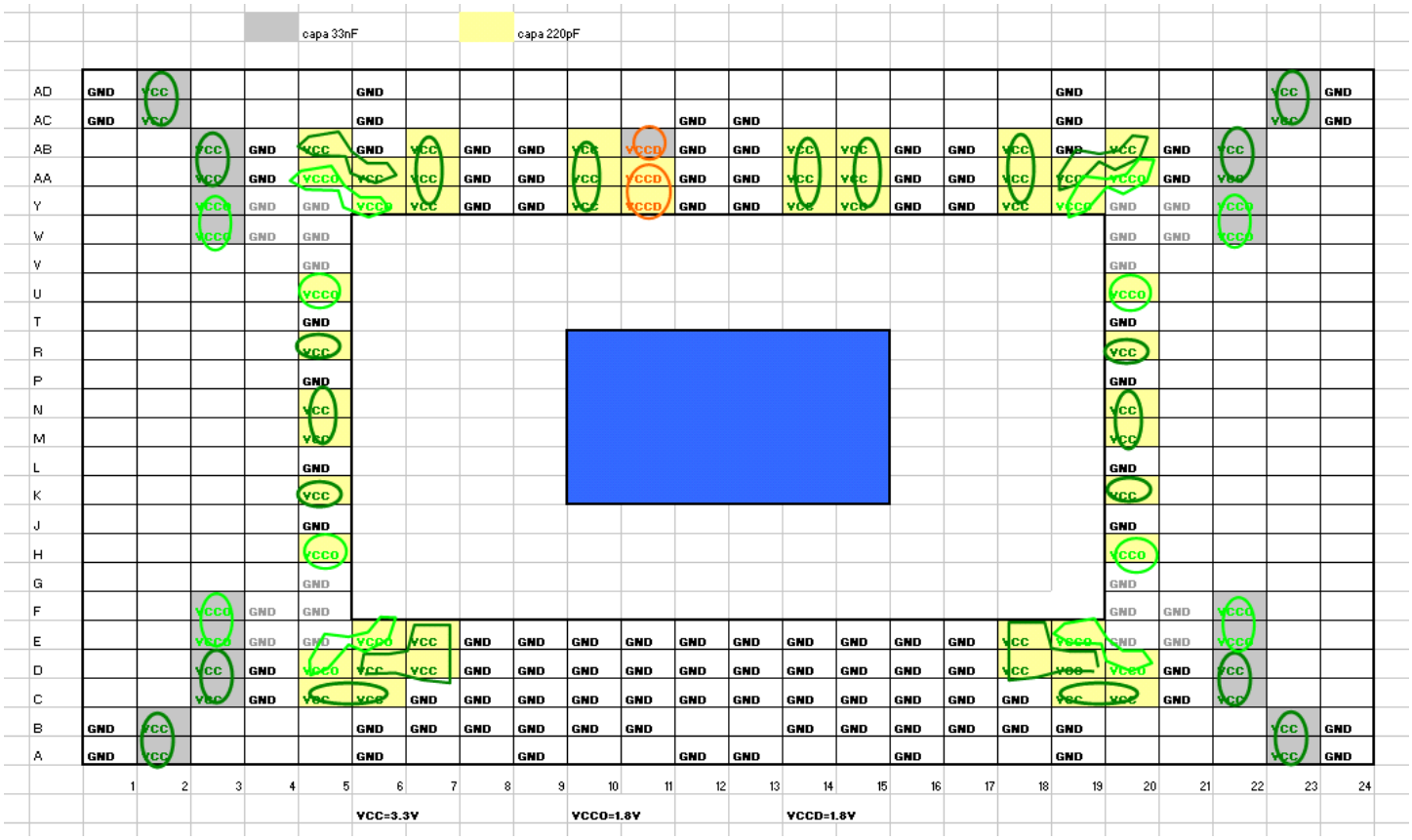
Figure 6-2. Power Supplies Decoupling Scheme



If the PCB space for decoupling capacitors is limited, adjustments to the value and number of capacitors can be made. The diagram below shows one such arrangement.

Figure 6-3. Suggested Power Supplies Decoupling Scheme



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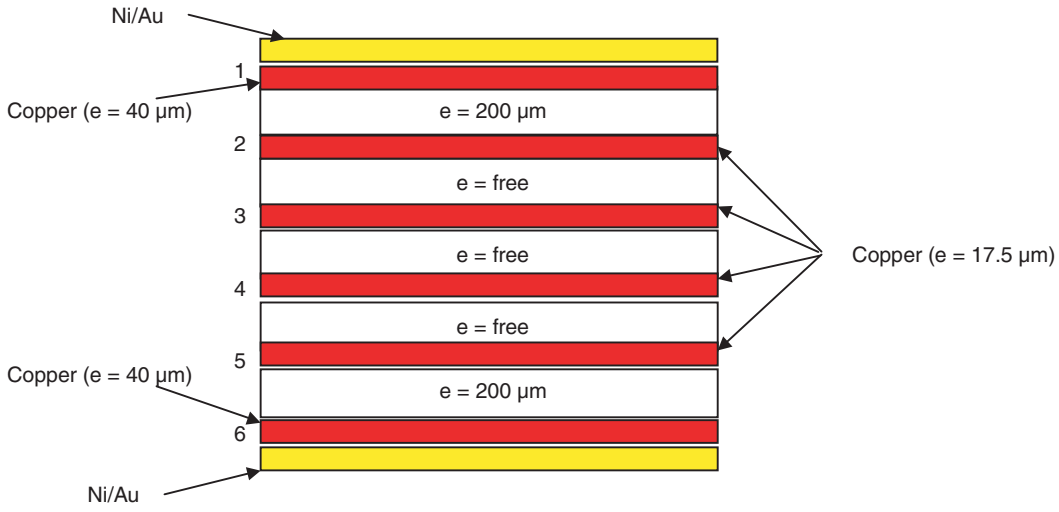
6.3 Board Layout Recommendations

6.3.1 PCB Stack Up

The recommended board stack up is described in Figure 6-4 on page 19. It applies to ISOLA410 PCB board material.

Figure 6-4. Board Recommended Stack Up Using ISOLA 410 Board Material



6.3.2 Clock, Analog Input And Output Data Signals

It is recommended to route the clock, analog input signals and output data signals as differential signals.

In the case of the use of a PCB with dielectric material such as FR4 HTG (ISOLA IS410 with 42% resin content and $\varepsilon t = 4$), the recommended board layout for the differential signals (clock and analog inputs) is described in Figure 6-5 and Figure 6-6 on page 20. This recommended layout only applies if the board stack up described in section Section 6.3.1 is satisfied.

Note: In the case of the digital output signals, the recommended differential routing is provided in Figure 6-6 on page 20.

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Figure 6-5 shows the standard routing with 1.27 mm pitch between signals of the same differential pair (clock and analog inputs only).

Figure 6-6 shows another possible routing for differential signals (clock analog inputs and digital outputs), preferred in case of high board size constraints.

Both configurations satisfy the impedance matching required for differential signals.

Figure 6-5. Differential Board Routing for The Clock and Analog Input Signals on FR4 HTG (IS410)

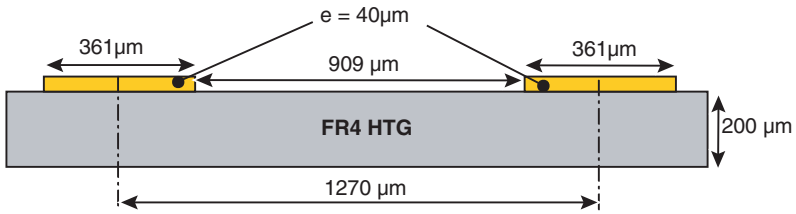
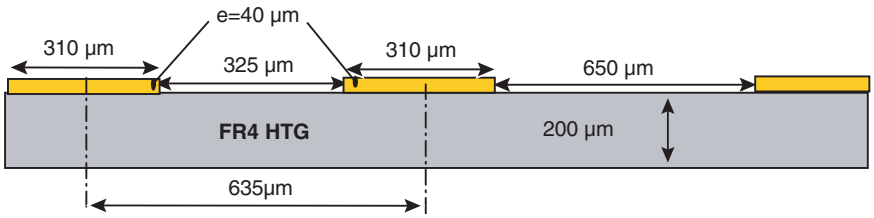
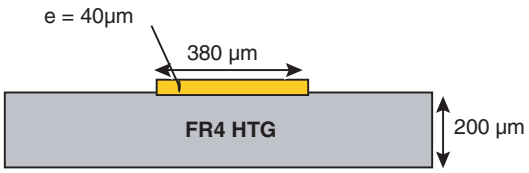


Figure 6-6. Differential Board Routing for the Clock, Analog Input and Digital Output Signals on FR4 HTG (IS410)



In the case of single-ended signals, the board layout should be as illustrated in Figure 6-7.

Figure 6-7. Single-ended Routing on FR4 HTG (IS410)



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How to reach us

Home page: www.e2v.com

Sales offices:

Europe Regional sales office

e2v ltd

106 Waterhouse Lane

Chelmsford Essex CM1 2QU

England

Tel: +44 (0)1245 493493

Fax: +44 (0)1245 492492

mailto: enquiries@e2v.com

e2v sas

16 Burospace

F-91572 Bièvres Cedex

France

Tel: +33 (0) 16019 5500

Fax: +33 (0) 16019 5529

mailto: enquiries-fr@e2v.com

e2v gmbh

Industriestraße 29

82194 Gröbenzell

Germany

Tel: +49 (0) 8142 41057-0

Fax: +49 (0) 8142 284547

mailto: enquiries-de@e2v.com

Americas

e2v inc

520 White Plains Road

Suite 450 Tarrytown, NY 10591

USA

Tel: +1 (914) 592 6050 or 1-800-342-5338,

Fax: +1 (914) 592-5148

mailto: enquiries-na@e2v.com

Asia Pacific

e2v ltd

11/F.,

Onfem Tower,

29 Wyndham Street,

Central, Hong Kong

Tel: +852 3679 364 8/9

Fax: +852 3583 1084

mailto: enquiries-ap@e2v.com

Product Contact:

e2v

Avenue de Rochepleine

BP 123 - 38521 Saint-Egrève Cedex

France

Tel: +33 (0)4 76 58 30 00

Hotline:

mailto: hotline-bdc@e2v.com

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